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Performance Analysis of DG FinFET for Ultralow-power Subthreshold Applications

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ABSTRACT

Subthreshold operating region of transistor shows huge potential toward satisfying demand of ultralow power (ULP) consumption from handheld portable devices. However, operating device with such small subthreshold leakage current as a switching current gives huge penalty in their operating frequency. For subthreshold operating region key design goal is to boost the speed of the device. DG FinFET device shows excellent device characteristics in subthreshold operating region. In this paper, 1-bit Full adder cell has been effectively analyzed. Since driving leakage current depends on operating temperature, performance analysis of Full adder is performed at different temperature. Simulation results show that dynamically connected static CMOS Full adder shows 43% advantage in delay over conv. static Full adder cell. DG FinFET-based Full adder cell shows significant advantage in delay as well as switching energy over static CMOS and DT CMOS-based Full adder.
Keywords: *Subthreshold, power-delay product, Dg FinFET, DTCMOS*

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INTRODUCTION

Subthreshold operating region shows huge prospective in fulfilling the ULP demand of portable devices having performance as secondary importance. It uses supply voltage less than the threshold voltage ($V_{DD} < V_{th}$). Previous research on subthreshold operation of Si-MOSFET shows that this operating region is more suitable for battery operated applications [1–3]. Thus, in future CMOS technologies we can expect prevailing importance of the subthreshold over superthreshold regime. However, due to utilization of leakage current as dynamic current, delay increases exponentially in subthreshold operating region. It is essential to increase the speed of such circuits to broaden its application area. Recently, while designing the low power circuits importance is given to operate the device at minimum energy delay point (EDP) shown in Figure 1 instead of MEP to achieve better speed.

Minimum EDP occurs in subthreshold operating region. The arithmetic unit is the fundamental block of any microprocessor, digital signal, and data processing architectures. Binary addition is considered as a central part of the arithmetic unit since all arithmetic operations generally involve addition. It is also a very decisive operation because it involves a carry propagation step and is the major speed limiting one. Improving the performance of Full adder directly leads to improving the performance of the whole system [4, 5].

The widely use of arithmetic function attracts a lot of research attention to build energy efficient Full adder design.

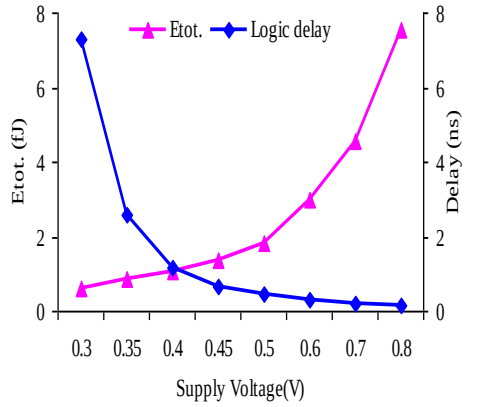

Fig. 1 E-D Curve for FO4 Test Bench.

This paper investigates the performance of 1-bit Full adder cell using conventional CMOS, DTCMOS, and most upcoming speed efficient DG FinFET devices. Rest of the paper is organized as follows. Section 2 introduced the subthreshold operating region. Section 3 explored 1-bit Full adder cell, Dynamic Threshold (DTCMOS) techniques, and DG FinFET device. Simulation results and performance comparison are carried out in Section 4. Section 5 draws the conclusion.

SUBTHRESHOLD OPERATING REGION

Subthreshold operating region uses small parasitic off-state subthreshold leakage current as switching current to realize the ULP circuits. This small leakage current can be expressed as follows [1],

$$I_D = I_0 e^{\frac{(V_{GS}-V_{th}+\eta V_{DS})}{nV_T}} \left(1 - e^{\frac{-V_{DS}}{V_T}}\right) \quad (1)$$

where V_{th} is the transistor threshold voltage, n the subthreshold slope factor ($n = 1 + C_d/C_{ox}$), V_T the thermal voltage, η the DIBL coefficient, and I_0 is the drain current at $V_{GS} = V_{th}$ @ $V_{DS} = V_{DD}$.

As gate leakage is strong function of V_{DD} it can be neglected due to low supply voltage for subthreshold operating region and use of high-*K* material in advanced technology. Other leakage components like direct tunneling gate leakage, gate induced drain leakage (GIDL), and reverse bias *p*–*n* junction leakage are also insignificant in subthreshold operating region.

BIT FULL ADDER CELL

Several logic styles have been used in the literature to design Full adder cells [6–8]. Each design style has its own merits and demerits. Traditional designs of Full adders usually employ only one logic style for the whole Full adder design. One example of such design is the standard static CMOS Full adder shown in Fig. 2. The 1-bit Full adder used is three inputs and two output blocks. This Full adder is based on regular CMOS structure with conventional pull-up and pull-down transistors providing full swing output. The main disadvantage of static CMOS circuits is the low mobility of its holes. The inputs are the two bits to be summed, A and B, and the carry bit Ci, which derives from the calculation of the previous digits. Schematic of 1-bit Full adder is as shown in Fig. 2. The outputs are the results of the sum operation S and the resulting value of the carry bit Co. Sum and carry output are given by [6],

$$S = A \oplus B \oplus C = \overline{A\,B\,Ci} + \overline{A}\,B\,\overline{Ci} + \overline{A\,B}\,Ci + A\,B\,Ci \quad (2)$$

$$Co = AB + (A + B)\,Ci. \quad (3)$$

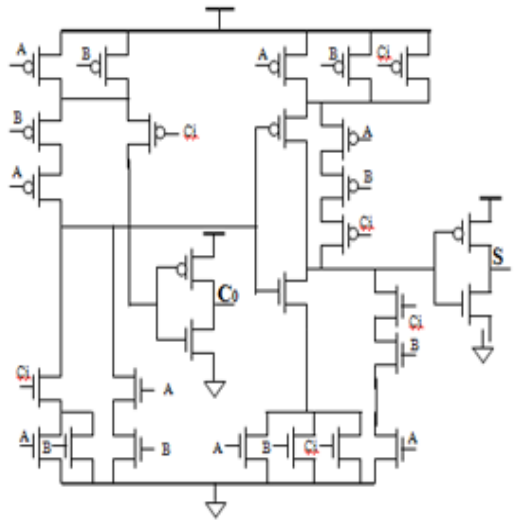

Fig. 2 1-Bit CMOS Full Adder Cell.

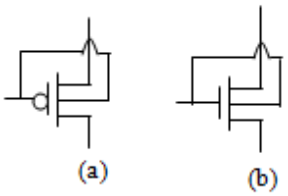

Fig. 3 Implementation of (a) DTPMOS, (b) DTNMOS.

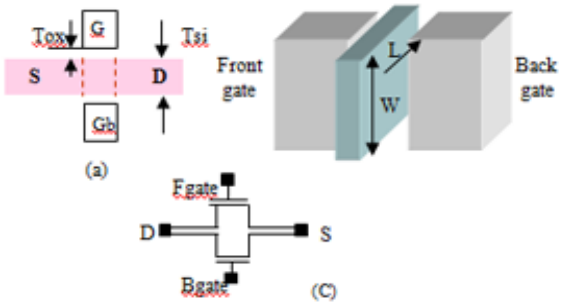

Fig. 4 The Structure of the Subcircuit Model of a FinFET Device: (a) Top View of Front and Back Gate; (b) Three-dimensional View; (c) Subcircuit Model [11].

DTMOS Full adder is implemented with transistors whose substrate and gate are tied together, as shown in Fig. 3 [9, 10]. The higher on current of DTMOS logic causes it to have higher power consumption; however, due to reduced threshold voltage delay reduces significantly. Sensitivity to the temperature variation can be reduced with the use of DTMOS structure.

Device structures based on silicon-on-insulator (SOI) technology have emerged as an effective means of extending MOS scaling beyond bulk limits for high- performance or low-power applications. The presence of double gate in FinFET structure provides better electrical properties as compared to the single gate MOSFET [11]. In 3T configuration front gate and back gate are shorted. Whereas, in 4T the back gate bias is fixed and front gate is acts for channel control. Furthermore, 3T and 4T configuration allows symmetric (3TSDG and 4TSDG) and asymmetric (3TADG and 4TADG) types of FinFET devices [12, 13]. In case of symmetric configuration both sub transistors of FinFET model as shown in Fig. 4(c) are having same device technology parameters. Asymmetric nature of the device can be obtained by using several ways; like using different front gate and back gate oxide thickness, different gate bias voltage, different threshold voltage, different gate material work functions, or by combination of all others. Figure 4(a) and (b) shows the transistor structure of FinFET. 3T symmetric configuration is having better driving current capabilities (lower delay) and higher power dissipation over 4T configuration.

SIMULATION RESULTS

Performance analysis of 1-bit Full adder is carried out using HSPICE simulator for 32 nm technology node. Predictive technology model file are used to simulate the CMOS Full adder [14]. As device sizing decides the performance characteristics we have optimized the same for optimum delay and power delay product (PDP) as shown in Fig. 5. Optimum PDP can be achieved at 3X minimum device size. Size of PMOS
transistor considered is 2X the size of NMOS transistor. Since operating temperature also affects the performance characteristics we have simulated the Figure 2 for two different temperatures at 25 and 85°C.

DTCMOS based and conventional Full adder performance is carried out at different supply voltage and different temperature. Figure 6 shows the delay comparison. As shown in Figure 6 dynamic threshold connected Full adder shows significant advantage in delay over conventional one. DTCMOS Full adder shows 43% advantage in delay at 25°C over conventional static Full adder at 0.3 V supply voltage. Static Full adder cell shows 13.8% at 85°C advantage over the same at 25°C. This is due to dependent of subthreshold leakage current on temperature. As temperature increases subthreshold leakage current increases. Figure 7 shows PDP comparison of dynamically threshold connected Full adder and conv. static Full adder. It is observed from PDP curves that DT connected Full adder is efficient in deep subthreshold region rather than in near threshold region. This is because operating DTMOS Full adder in near threshold region increases power dissipation hence results increases PDP significantly. Figures 8 and 9 show simulation waveforms for functional verification of CMOS and DG FinFET at 0.35 V supply voltage. Table I shows comparison of Full adder performance parameters at different temperatures in subthreshold region and Table II shows the same for superthreshold operating region. It is observed from the Tables I and II that subthreshold Full adder is more power efficient due to reduced supply voltage. However, it gives significant penalty in delay. FinFET-based Full adder improves speed of Full adder of order of magnitude. Delay of static CMOS-based Full adder decreases with increase in temperature, and that of FinFET Full adder increases with temperature.

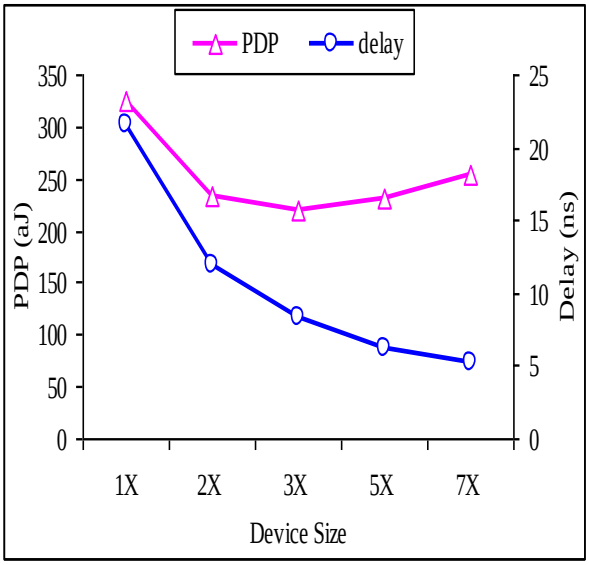

Fig.5 Effects of Device Sizing on Full Adder Performance.

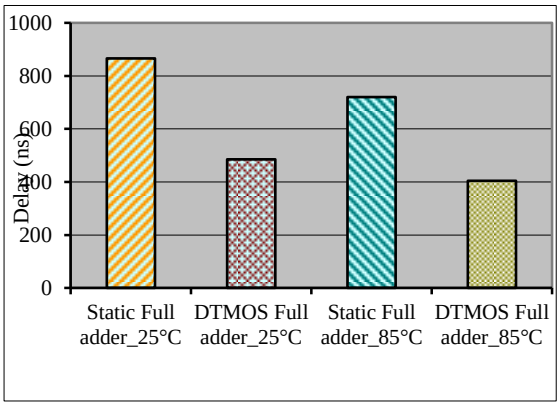

Fig.6 Delay Comparison for Full Adder Cell at Different Temperature.

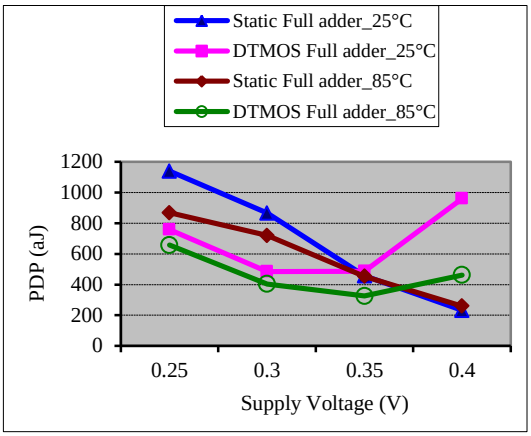

Fig. 7 PDP Comparison for Full Adder Cell at Different Temperature.

Table I Comparison of CMOS and FinFET Full Adder Cell at VDD = 0.22V.

	T=25° C			T=85° C		
	Delay (ps)	*Pav (nW)*	*PDP (aJ)*	*Delay (ps)*	*Pav (nW)*	*PDP (aJ)*
CMOS	340	47.37	16.14	484.99	53.93	26.15
FinFET (Symmetric)	18.65	313	5.84	18.55	187	3.47

Table II Comparison of CMOS and FinFET Full Adder Cell at VDD = 0.9 V.

	T = 25°C			*T* = 85°C		
	Delay (ns)	Pav (nW)	PDP (aJ)	Delay (ns)	Pav (nW)	PDP (aJ)
CMOS	407	0.62	253	272	1.01	276
DTCMOS	71.11	2.3	164	42.46	3.61	153
FinFET (Symm.)	1.59	4.63	7.39	3.59	2.35	8.45
FinFET (Asy.)	4.68	4.08	19.14	12.79	1.95	24.96

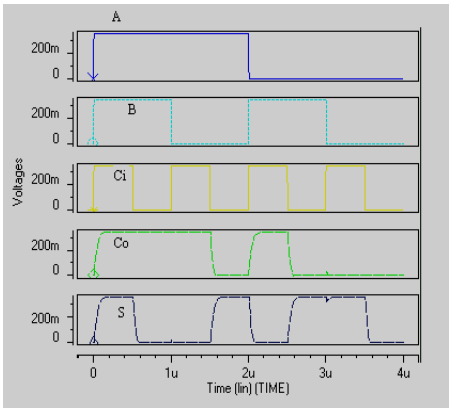

Fig. 8 Simulation Waveform for Functional Verification of Full Adder Conv. CMOS at 0.35 V.

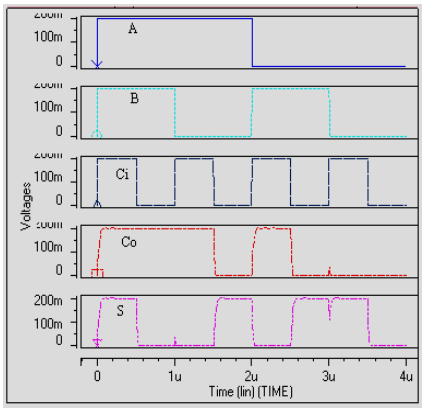

Fig. 9 Simulation Waveform for Functional Verification of Full Adder DG FinFET at 0.2 V.

EFFECT OF PROCESS PARAMET ER VARIATION ON DG FINFET PARFORMANCE

In this section, FinFET with different fin thickness and gate oxide thickness are designed and characterized for minimum delay and energy-delay product. HSPICE compatible equivalent DG-FinFET subcircuit model simulated at the 32 nm technology node. The fin thickness is varied from 5 to 10 nm and front and back gate oxide thickness is varied from 0.8 to 1.8 nm. Test bench shown in Fig. 2 is simulated with HSPICE under subthreshold region. Figures 10 and 11 show delay and energy delay product as a function of tsi and tox, respectively. It has been observed from Fig. 10 that at tox = 1.6 nm and tsi = 5nm 1-bit full adder cell is minimum delay performance. Increasing the tox by 20% on current (subthreshold leakage current) increases by 13% it is due to short channel devices large change in drive current due to toxvariation. Also parasitic capacitances start dominating the intrinsic capacitance and Ioff current increases by 16.91% for 20% which results increase in circuit delay. Similar energy delay product trend is observed as shown in Fig. 11 for different values of tsi and tox. The impact of supply voltage and temperature variation on a FinFET-based static full adder is characterized in Figs. and Fig. 13. Increasing temperature and decreasing supply voltage increases the delay.

Figures 12 and 13 also shows that using optimum tsi and tox for subthreshold region significant improvement in delay and energy delay product can be obtained. It has also been observed that oscillation frequency and power dissipation decreases on supply voltage scaling. Hence, depending upon application's requirement it is necessary to select proper value of operating voltage. Figure 10 shows effect of tsi variation on ring oscillator's frequency. Ring oscillator with tsi = 5 nm shows 10% improvement in oscillation frequency than over tsi = 10 nm.

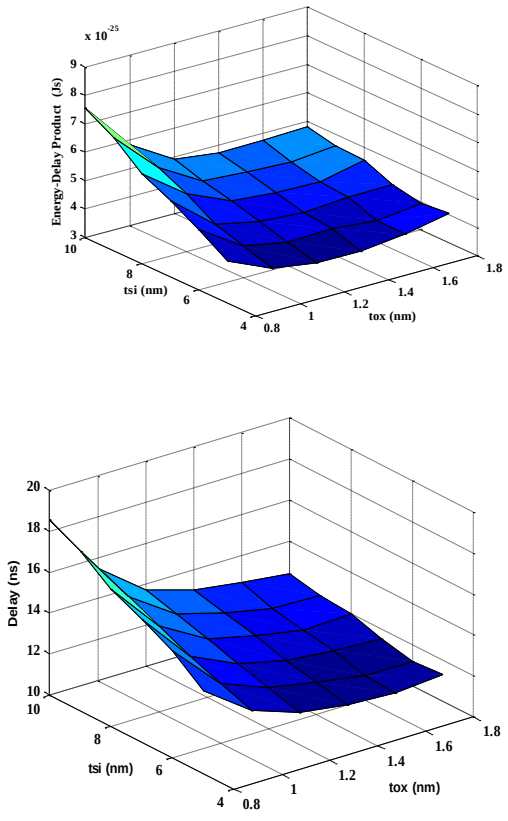

Fig. 11 Energy-Delay Product as Function of tsi and tox.

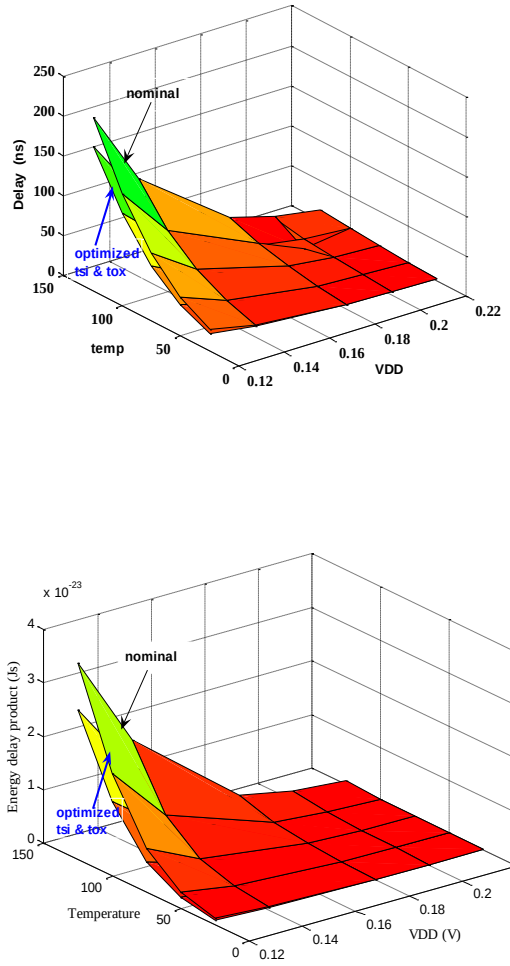

Fig. 12 Delay as Function of Temperature and V_{DD}.

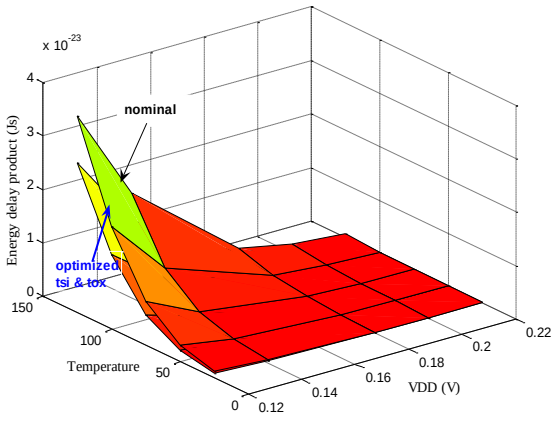

Fig. 13 Energy-Delay Product as Function of Temperature and V_{DD}.

CONCLUSION

Subthreshold operation of device is most promising approach to offer ultralow power circuits. However, it gives huge amount of delay penalty. Improving the speed of subthreshold circuits will expand the application area. This paper put efforts toward performance analysis of 1-Full adder cell under subthreshold operating conditions for power efficient circuits. DG FinFET shows better candidate for subthreshold Full adder. DG FinFET-based Full adder shows significant advantage in delay over conv. static CMOS-based Full adder. DTMOS technique shows better advantage in deep subthreshold region than the near threshold operating region.

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