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Adaptive-Hysteresis Current Controller Based Shunt Active Power Line Conditioners for Power Quality Improvements

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ABSTRACT

This paper presents three-phase shunt active power line conditioners (APLC) for harmonics and reactive power compensation due to non-linear loads in the distribution network. The compensation process proposed is a sinusoidal extraction control method, which consists of positive-sequence voltage detector for regulating the supply voltage and instantaneous reactive power (p-q) theory for fundamental extraction from the distorted line current. The shunt active filter voltage source inverter's switching pulses are generated through an adaptive-hysteresis current controller (HCC). The adaptive-hysteresis bandwidth can be adjusted based on compensation current variation that is used to optimize the required switching frequency. This will improve the active power filter performance. The shunt-APLC system is validated through extensive simulation under steady and transient states with non-linear load conditions.

Keywords: *Active power line conditioners (APLC), sinusoidal extraction controller, positive-sequence voltage detector, p-q theory, adaptive-hysteresis current controller (HCC)*

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INTRODUCTION

Of late, a lot of research is being conducted for power quality and custom power problems due to the non-linear loads in the power transmission and distribution systems [1]. In practical application, most of the loads are of non-linear characteristics, such as power converters, arc furnaces, UPS, ASDs, etc. These non-linear loads introduce harmonic distortion, and reactive power problems [2]. The harmonics in the system induce several issues such as increased heating losses in transformers, low power factor, torque pulsation in motors, poor utilization of distribution plant and affect other loads connected at the same point of common coupling (PCC) [3–5]. Traditionally, passive L-C filters were used to mitigate line harmonics; however, these filters have demerits of aging and tuning problems, resonance, bulk size, and also fixed compensation [6]. Over the last twenty-five years, active power filters (APFs) or active power-line conditioners (APLCs) have been developed for compensating the harmonics and reactive power simultaneously [7]. An APF has the ability to keep the mains current balanced and sinusoidal after compensation, regardless of whether the load is under non-linear and/or balanced/unbalanced conditions [8].

The controller is the most significant part of the active power filter and currently different control strategies are proposed by different researchers [6–8]. There are various control strategies such as instantaneous reactive power theory, synchronous reference frame theory, Fryze current minimization method, genetic algorithm, and notch filter, which are proposed

to extract the harmonic components [9–12]. The proposed sinusoidal extraction control algorithm is most suitable for active filter design. Because of simple mathematical calculation, robustness, and good dynamic response [14,15], this controller contains positive sequence voltage detector and instantaneous reactive power theory (p-q theory) concept. The basis of p-q theory is providing good compensation characteristics [2]. The current harmonics principle is accomplished with active power filter by injecting equal but opposite current harmonic components at the point of common coupling (PCC), thereby canceling the original harmonic and improving the power quality on the connected distribution system [16, 17].

Similarly, various current control techniques are proposed for the APF controller such as a triangular current controller, sinusoidal PWM, periodical sampling controller, discrete PWM, and hysteresis current controller [18, 19]. Nowadays, the hysteresis current controller method attracts researchers' attention due to unconditional stability, fast transient response, simple implementation, and high accuracy [19]. However, this control scheme exhibits several unsatisfactory features such as uneven switching frequency and the switching frequency varies within a particular band limit only [20, 21]. The adaptive hysteresis current controller overcomes these HCC dermatitis; adaptive-HCC changes the bandwidth according to instantaneous compensation current variation. This controller is maintaining the modulation frequency constant; that will improve the PWM performances and makes APF substantially [22, 23].

This paper presents a sinusoidal extraction controller-based shunt APLC for current harmonics and reactive power compensation under non-linear loads. The shunt active filter is implemented with voltage source inverter and switching signals are derived from hysteresis current controller. The shunt APLC is investigated and measured against various parameter values under distorted supply voltage and non-linear load conditions.

SINUSOIDAL EXTRACTION CONTROL STRATEGY

The sinusoidal extraction control strategy is used to extract the reference current or fundamental components from the distorted line (harmonic load) current. This controller contains positive sequence voltage detector and instantaneous reactive power concept. The distorted voltage sources Vsa, Vsb and Vsc perform with the positive sequence voltage detector and generate balanced instantaneous sinusoidal voltages

Positive Sequence Voltage Detector

Figure 1 shows the block diagram of the positive-sequence voltage detector that consists of two major parts – one is PLL circuit and the other is instantaneous power calculation (p-q theory). The voltage sources Vsa, Vsb and Vsc

are transformed into the $\alpha\beta$ coordinates to determine v_α *and* v_β . Using Clarke transformation, it can be written as

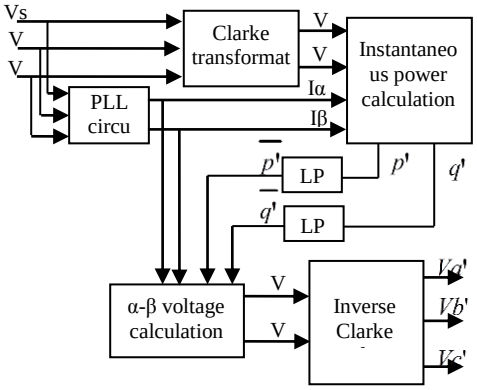

Fig. 1 Positive Sequence Voltage Detector.

$$\begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \quad (1)$$

They are used to meet with auxiliary currents i_α' *and* i_β' that are produced from the PLL-synchronizing circuit. To calculate the auxiliary powers p' *and* q' from the $\alpha\beta$ coordinate voltages and PLL-circuit output,

$$p' = v_\alpha\, i_\alpha' + v_\beta\, i_\beta' \quad (2)$$

$$q' = v_\beta\, i_\alpha' + v_\alpha\, i_\beta' \quad (3)$$

the auxiliary powers p' *and* q' are passed through first order Butterworth design-based 50 Hz low pass filter (LPF) to eliminate the higher order components; it allows the fundamental components only. The LPF obtains the average powers $\bar{p}'$ *and* $\bar{q}'$. The instantaneous voltages v_α' *and* v_β' which correspond to time functions of the fundamental positive sequence voltage detector of the system, can be derived as

$$\begin{pmatrix} v_\alpha' \\ v_\beta' \end{pmatrix} = \frac{1}{(i_\alpha')^2 + (i_\beta')^2} \left\{ \begin{pmatrix} i_\alpha' & i_\beta' \\ i_\beta' & -i_\alpha' \end{pmatrix} \begin{pmatrix} \bar{p}' \\ \bar{q}' \end{pmatrix} \right\} \quad (4)$$

The instantaneous three-phase voltages va', vb' *and* vc' can be calculated from the $\alpha\beta$ coordinate voltages v_α' *and* v_β' . By applying the inverse Clarke transformation, it can be derived as

$$\begin{pmatrix} va' \\ vb' \\ vc' \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} v_{\alpha'} \\ v_{\beta'} \end{pmatrix} \quad (5)$$

The positive sequence voltage detector provides good dynamic and accurate results even under distorted or unbalanced conditions. This controller makes the shunt active filter to compensate load currents, so that only the active portion of the fundamental positive sequence component, which produces average real-power only, is supplied by the source. The PLL circuit must provide auxiliary currents to sinusoidal functions at the fundamental frequency. The next part presents a PLL-circuit working process.

Phase Locked Loop (PLL) Circuit

The PLL circuit consists for operate under distorted and unbalanced supply voltage. The block diagram of a PLL circuit is shown in Figure 2. This algorithm is based on the three-phase instantaneous active power expression. It can be expressed as $p_{3\phi} = v_a i_a + v_b i_b + v_c i_c$.

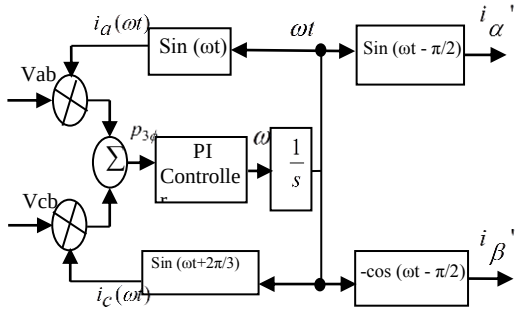

Fig. 2. A PLL Circuit.

The $i_c(\omega t) = \sin(\omega t + 2\pi/3)$ are built up by the PLL circuit and time integral ω is calculated using a proportional-integral controller. The PLL circuit can reach a stable point when the input $p_{3\phi}$ of the PI-controller has a zero average value ($p_{3\phi} = 0$) and has minimized low-frequency oscillating portions in three-phase voltages. Once the circuit is stabilized, the average value of $p_{3\phi}$ is zero and the phase angle of the supply voltage is at fundamental frequency. At this condition, the currents become orthogonal to the fundamental phase voltage component. The PLL synchronizing output currents are defined as

$$i_\alpha' = \sin(\omega t - \pi/2) \quad (6)$$

$$i_\beta' = -\cos(\omega t - \pi/2) \quad (7)$$

The PLL design should allow proper operation under distorted supply voltages. The PLL synchronizing output currents are used to determine the instantaneous auxiliary powers p' *and* q' calculation.

Instantaneous Reactive-Power Theory

Figure 3 shows the block diagram of the sinusoidal extraction control strategy. It has two important parts – one is positive sequence voltage detector to generate the balanced sinusoidal voltage va', vb' *and* vc' from distorted or unregulated supply voltages Vsa, Vsb *and* Vsc, which was explained before this section. This section explains about the instantaneous reactive-power theory for extract the reference current from the distorted line current.

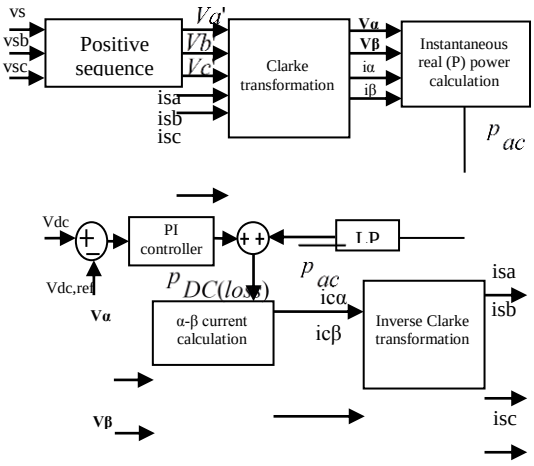

Fig.3 Block Diagram of the Sinusoidal Extraction Controller.

The instantaneous *abc* coordinate and sinusoidal voltage va', vb' *and* vc' are transformed into the $\alpha\beta$ coordinate voltages by using the Clarke transformation. It can be written as

$$\begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} v_a' \\ v_b' \\ v_c' \end{pmatrix} \quad (8)$$

Similarly, the instantaneous source current isa, isb *and* isc also transforms into the $\alpha\beta$ coordinate current i_α, i_β by Clarke transformation,

$$\begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{pmatrix} \quad (9)$$

where α and β axes are the orthogonal coordinates. The voltage v_α and current i_α are on the α -axis and v_β *and* i_β are on the β -axis. Let the instantaneous real power calculated from the α -axis and the β -axis of the current and voltage respectively. They are given by the conventional definition of real-power as follows:

$$p_{ac} = v_\alpha \, i_\alpha + v_\beta \, i_\beta \quad (10)$$

The instantaneous real-power (p_{ac}) passes through Butterworth design-based LPF. The LPF cutoff frequency is 50 Hz that allows only the fundamental signal to the active power section that calculates the AC components of the real power losses and it is denoted as $\overline{p_{ac}}$

The DC power loss is calculated from the comparison of the dc-side capacitor voltage of the inverter and the desired reference voltage. The proportional integral controller determins the dynamic response and settling time of the dc-side voltage. The DC component power losses can be written as

$$p_{DC(loss)} = \left[v_{DC,ref} - v_{DC} \right] \left[k_P + \frac{k_I}{s} \right] \quad (11)$$

The instantaneous real power (p) is calculated from the AC component real power losses $\overline{p_{ac}}$ and the DC power losses $p_{DC(Loss)}$); it can be defined as follows:

$$p = \overline{p_{ac}} + p_{DC(Loss)} \quad (12)$$

The AC and DC components of the instantaneous power p are related to the harmonic compensation currents. The instantaneous real power generates the required reference currents to compensate the current harmonics and reactive power. The instantaneous current on the $\alpha\beta$ coordinates of $i_{c\alpha}$ *and* $i_{c\beta}$ are divided into two kinds of instantaneous current components – the first is real-power loss and the other reactive power loss – but this proposed controller computed only the real power losses. The $\alpha\beta$ coordinate currents $i_{c\alpha}, i_{c\beta}$ are calculated from the v_α , v_β voltages with instantaneous real power p and the reactive power q is assumed as zero. This approach reduces the calculations and result in better performance than the conventional methods; the $\alpha\beta$ coordinate currents can be calculated as

$$\begin{pmatrix} i_{c\alpha} \\ i_{c\beta} \end{pmatrix} = \frac{1}{v_\alpha^{\,2} + v_\beta^{\,2}} \left\{ \begin{pmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{pmatrix} \begin{pmatrix} \overline{p} + p_{(loss)} \\ 0 \end{pmatrix} \right\} \quad (13)$$

The references of the compensating currents are calculated instantaneously without any time delay by using the instantaneous $\alpha\beta$ - coordinate currents. The desired reference currents derivate from the inverse Clarke transformation and can be written as

$$\begin{pmatrix} i_{sa}^{*} \\ i_{sb}^{*} \\ i_{sc}^{*} \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} i_{c\alpha} \\ i_{c\beta} \end{pmatrix} \qquad (14)$$

The small amount of real power is adjusted by changing the amplitude of fundamental component of reference current; the objective of this algorithm is to compensate all undesirable components. The control strategy indicates that shunt APF should draw the inverse of the non-active current of the load and the results show that compensated currents are proportional to the corresponding phase voltage. When the power system voltages are balanced and sinusoidal, it leads to constant power at the dc-side capacitor voltage of the inverter. The next section explains different current control strategies for generating gate

control switching pulses to voltage source inverter.

ADAPTIVE-HYSTERESIS CURRENT CONTROLLER

The reference currents $(i_{sa}^{*}, i_{sb}^{*} \text{ and } i_{sc}^{*})$ compare with actual source current $(i_{sa}, i_{sb} \text{ and } i_{sc})$ and generate inverter switching pulses using the adaptive-hysteresis current controller [20]. The adaptive-HCC changes the hysteresis bandwidth based on instantaneous compensation current variation to optimize the required switching frequency [21, 22]. Figure 4 shows the inverter of the current and voltage waves for phase a . The current i_a tends to cross the lower hysteresis band at point 1, where the inverter switch S1 is switched ON. The linearly rising current $(i_a +)$ then touches the upper band at point 2, where the inverter switch S4 is switched ON. The linearly falling current $(i_a -)$ then touches the lower band at point 3.

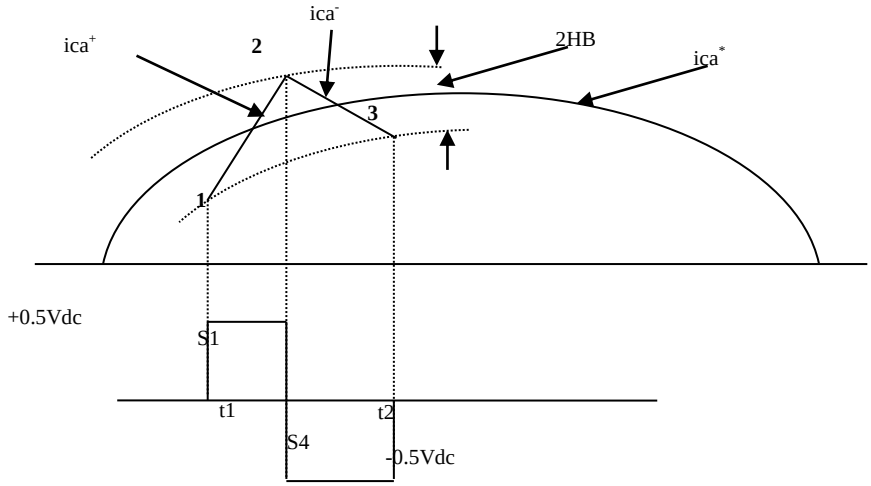

Fig. 4 Current and Voltage Waves with Adaptive HCC.

The following equations can be written in the switching intervals t_1 and t_2

$$\frac{di_{ca}^{+}}{dt} = \frac{1}{L}(0.5V_{dc} - V_{sa}) \quad (15)$$

$$\frac{di_{ca}^{-}}{dt} = -\frac{1}{L}(0.5V_{dc} + V_{sa}) \quad (16)$$

where $L =$ phase inductance; $(i_a +)$ and $(i_a -)$ are the respective rising and falling current segments.

From the geometry of Figure 4, we can write

$$\frac{di_{ca}^{+}}{dt}t_1 - \frac{di_{ca}*}{dt}t_1 = 2HB \quad (17)$$

$$\frac{di_{ca}^{-}}{dt}t_2 - \frac{di_{ca}*}{dt}t_1 = -2HB \quad (18)$$

$$t_1 + t_2 = T_c = 1/f_c \quad (19)$$

where t_1 and t_2 are the respective switching intervals, and f_c is the modulation frequency. Adding Eqs. 17 and 18and substituting (19) we can write

$$\frac{di_{ca}^{+}}{dt}t_1 - \frac{di_{ca}^{-}}{dt}t_2 - \frac{1}{f_c}\frac{di_{ca}^{*}}{dt} = 0 \quad (20)$$

Subtracting Eq. (18) from (17), we get

$$\frac{di_{ca}^{+}}{dt}t_1 - \frac{di_{ca}^{-}}{dt}t_2 - (t_1 - t_2)\frac{di_{ca}^{*}}{dt} = 4HB \quad (21)$$

Substituting Eq. (16) in (21) , we get

$$\frac{di_{ca}^{+}}{dt}(t_1 + t_2) - (t_1 - t_2)\frac{di_{ca}^{*}}{dt} = 4HB \quad (22)$$

Substituting Eq. (16) in (20) , and simplifying,

$$(t_1 - t_2) = \frac{di_{ca}^{*}/dt}{f_c(di_{ca}^{+}/dt)} \quad (23)$$

Substituting Eq. (23) in (22) it gives,

$$HB = \left\{\frac{0.125V_{dc}}{f_c L}\left[1 - \frac{4L^2}{V_{dc}^{\ 2}}\left(\frac{V_{sa}}{L} + m\right)^2\right]\right\} \quad (24)$$

Here, $m = di_a^{*}/dt$ is the slope of reference current signals. The hysteresis band HB can be modulated at different points of fundamental frequency cycle to control the switching pattern of the inverter. The calculated hysteresis bandwidth HB is applied to the variable HCC. The variable HCC created by s-functions in Matlab produce gate control pulses and these pulses operate the voltage source inverter

SIMULATION RESULT AND ANALYSIS

The performance of the proposed sinusoidal extraction control and adaptive-HCC method-based shunt APLC is evaluated through Matlab/Simulink power system. The model system consists of a three-phase distorted supply voltage with a rectifier R-L load. The active filter is connected to the distribution system at PCC through an inductor. The active filter comprises of six power transistors with power diodes, a dc-capacitor, an RL-filter, a compensation controller (sinusoidal extraction controller), and a switching pulse generator (adaptive-HCC) shown in Figure 5. The values

of the circuit elements used in simulation are given in Appendix-A.

The system is tested under distorted supply voltages. Figure 6 (a) indicates three-phase distorted source voltages. These distorted voltages are involved with the positive sequence voltage detector and generate balanced (regulated) instantaneous sinusoidal voltages. Figure 6 (b) shows balanced sinusoidal voltages; these waveforms are extracted from the distorted voltages waveform.

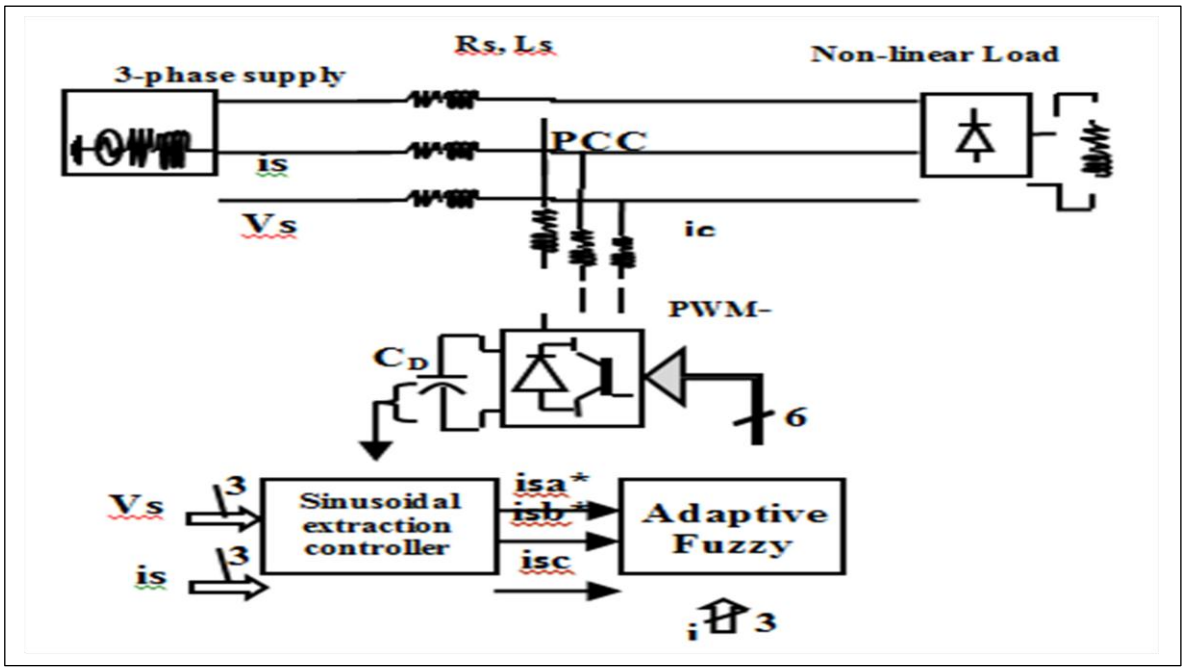

Fig. 5 Block Diagram of APLC System.

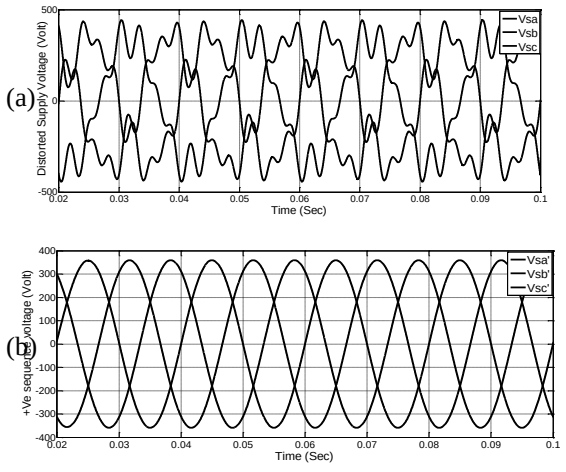

Fig. 6 Simulation Results (a) Distorted Supply-Voltage and (b) Output of Positive Sequence Voltage.

The source currents are drawing non-sinusoidal or non-linear characteristics waveform due to the non-linear load. These non-linear load currents contain fundamental and harmonic components, which can be represented as

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \Phi_n)$$

$$= I_1 \sin(\omega t + \Phi_1) + \left(\sum_{n=2}^{\infty} I_n \sin(n\omega t + \Phi_n) \right) \quad (25)$$

The six-pulse diode rectifier R-L load current waveform is shown in Figure 6 (c). Here, active power filter is absent, so the source current is drawing non-sinusoidal current waveforms.

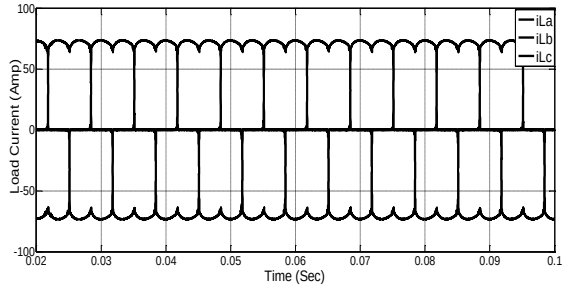

Fig. 6 (c) Source Currents before Compensation.

The instantaneous load power can be multiplied from the source voltage and current. It can be represented as

$$\begin{aligned} p_L(t) &= i_s(t) * v_s(t) \\ &= V_m \sin^2 \omega t * \cos\varphi_1 + V_m I_1 \sin \omega t * \cos \omega t * \sin \varphi_1 \\ &\quad + V_m \sin \omega t * \left(\sum_{n=2}^{\infty} I_n \sin(n\omega t + \Phi_n) \right) \\ &= p_f(t) + p_r(t) + p_h(t) \end{aligned} \quad (26)$$

This load power contains fundamental (or real power) $p_f(t)$, reactive power $p_r(t)$ and harmonics power $p_h(t)$. From this equation, only the active (fundamental) power drawn by the load is

$$p_f(t) = V_m I_1 \sin^2 \omega t * \cos\varphi_1 = v_s(t) * i_s(t) \quad (27)$$

If the active power filter provides the total reactive and harmonic power, the source current will be sinusoidal. At this time, the active filter must provide the compensation current

$$i_c(t) = i_L(t) - i_s(t) \quad (28)$$

The active filter provides the compensating current to eliminate the harmonics that is shown in Figure 6 (d).

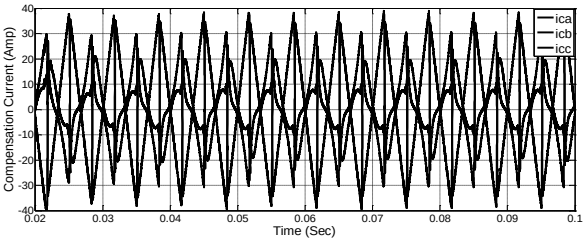

Fig. 6 (d) Compensation Current.

From Eq. (19), the source current drawn from the AC mains after compensation should be sinusoidal; this is represented as

$$i_s(t) = p_f(t) / v_s(t) = I_1 \cos\varphi_1 \sin \omega t = I_{\max} \sin \omega t \quad (29)$$

The active power filter keeps the mains current balanced and sinusoidal after compensation. The performance of the active filter with the proposed control algorithm is proof that the source current became sinusoidal that is shown in Figure 6(e).

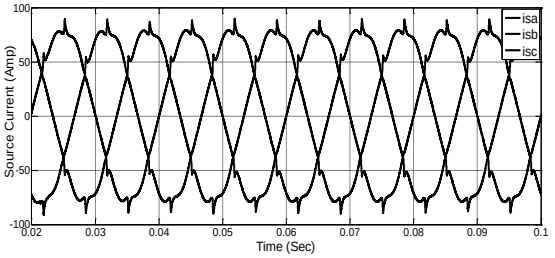

Fig. 6(e) Source Current after Compensation Filter.

We have additionally achieved power factor correction as shown in Figure 6 (f) that indicates the voltage and current are in phase.

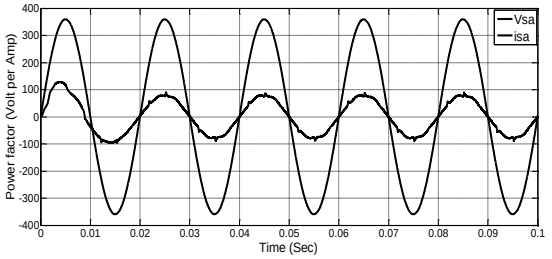

Fig. 6 (f) Unity Power Factors.

For transient, the steady state suddenly changes to transient condition using step-size at T=0.06/0.12s. The load current is shown in Figure 7 (a) that contains fundamental and harmonic components. The APF supplies the compensating current that is shown in Figure 7 (b). The source current after compensation is presented in Figure 7 (c) that indicates the current becomes sinusoidal.

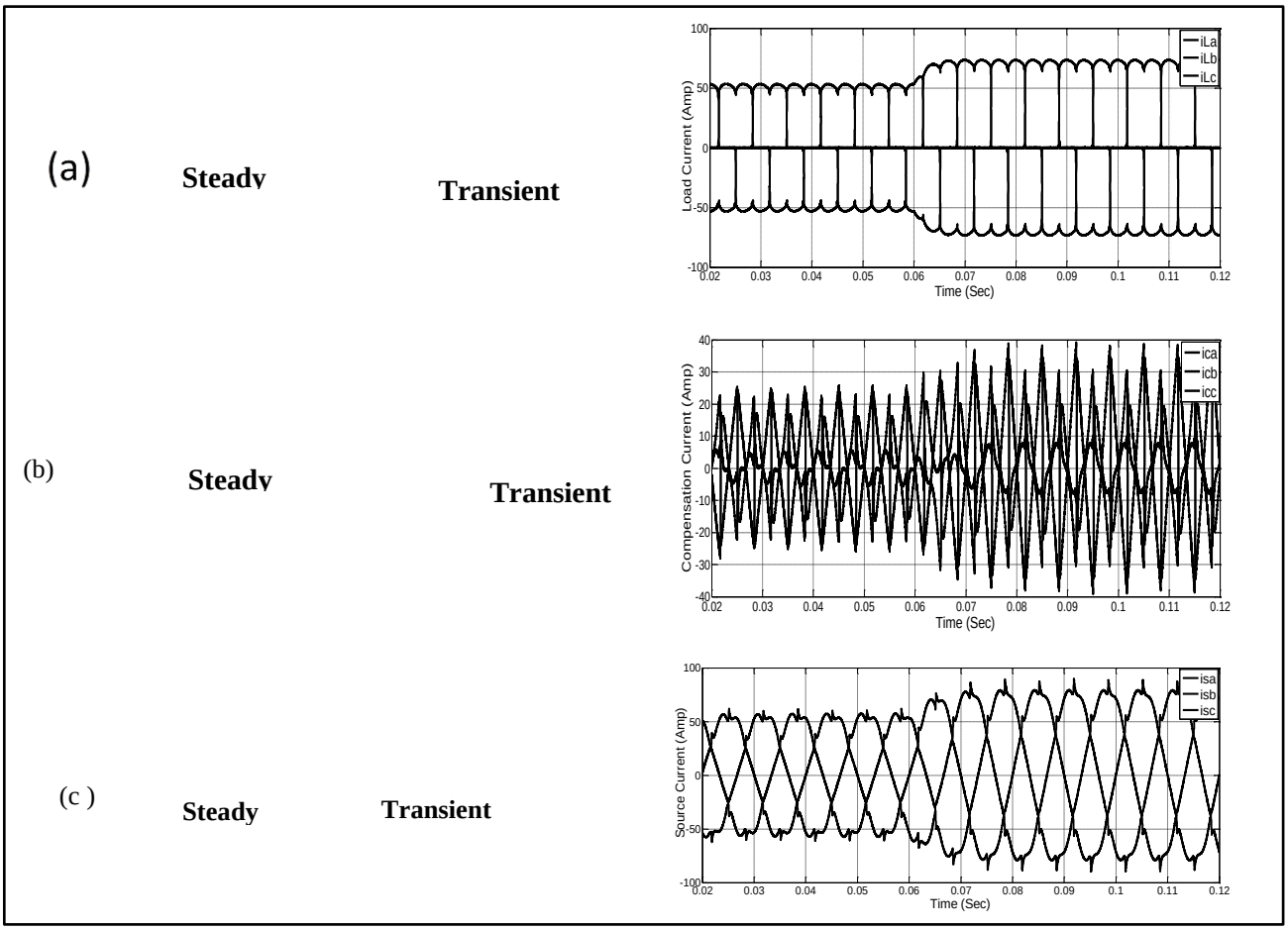

Fig. 7 Transient State (a) Load Currents, (b) Compensation Current by APF, (c) Source Current after Compensation.

The switching frequency of the inverter depends on the dc-side capacitor voltage. It maintains constant with less settling time by proposed controller. Figure 7 (d) shows the dc-side capacitance voltage of the inverter settling time measured under transient state (t=0.02s).

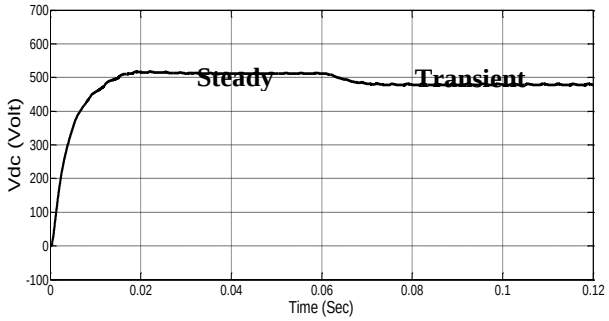

Fig. 7 (d) DC-Side Capacitor Voltage Settling Times.

The fast fourier transform (FFT) is used to measure the order of harmonics with the fundamental frequency 50 Hz at the source current. These orders of the harmonics are plotted in Figure 8 (a), without and with active power filter in Figure 8 (b). From the result, we can observe that sinusoidal extraction controller-based shunt APLC is compensating the harmonics effectively.

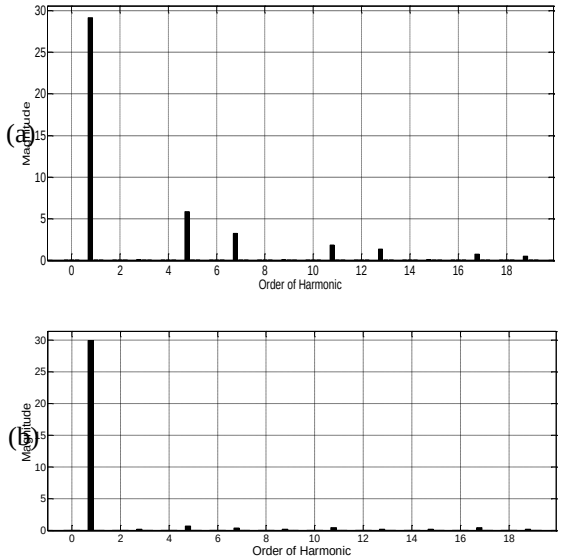

Fig. 8 Order of Harmonics (a) the Source Current without Active Filter (b) with Active Power Filter.

The total harmonic distortion is measured from source current on the ac main network. The sinusoidal extraction controller-based compensator filter made sinusoidal source current in the supply. The total harmonic distortion measured with or without active power filter are presented in Table I.

Table I FFT Analysis of THD.

Condition(THD)	**Without APF**	**With APF**
Steady State	26.67%	4.21%
Transient	24.89%	3.76%
Power Factor	0.9578	0.9995

The real (P) and reactive (Q) powers are calculated and given in Table II. This result is measured under non-linear load condition using adaptive-hysteresis controlled shunt APF system. This result indicates that the active power filter is suppressing the reactive power and improves the power quality in the distribution system at PCC.

Table II Real (P) and Reactive (Q) Power Measurement.

Conditionz	**Real (P) and Reactive (Q) Power Measurement**	
	Without APF	**With APF**
Steady State	P = 10.11 kW Q = 267 VAR	P = 10.87 kW Q = 024 VAR
Transient State	P = 13.18 kW Q = 398 VAR	P = 13.96 kW Q = 086 VAR

The simulation is done with distorted supply voltage with non-linear load conditions. The obtained result shows that the source current and load current show small variation in steady state and transient conditions. The FFT analysis of the active filter brings the THD of the source current to less than 5% when adopted into IEEE 519 and IEC 61000-3 standards.

CONCLUSIONS

The proposed sinusoidal extraction controller for three-phase shunt active power line conditioners facilitates current harmonics reduction and reactive power compensation due to the non-linear loads. The distorted supply voltages are regulated by positive-sequence voltage detector and harmonic currents are extracted using p-q theory; the attempt is different from the conventional methods. The active filter voltage source inverter switching signals are generated from adaptive-hysteresis band current controller. The obtained result shows the source current and load current is small variation in steady state and transient conditions. The measured total harmonic distortion of the source currents is in compliance with IEEE 519 and IEC 61000-3 harmonic standards under non-linear loads. This proposed sinusoidal extraction control algorithm-based APLC system can be implemented in field programmable gate array (FPGA) devices as a future work.

APPENDIX-A

Table III System Parameters.

Parameters	**Values**
Line to Line Source Voltage (Vm)	440 V
System Frequency (f)	50 Hz
Source Impedance: Source Resistor (R_S) Source Inductor (L_S)	0.1 Ω 0.1 mH
Non-Linear Load: Load Resistor (R_L) Load Inductor (L_L)	6-Diode Rectifier 20 Ω 100 mH
Unbalanced Load: Load Inductor (L_L) Load Resistor (R_L)	10 mH 10 Ω, 50 Ω, 90 Ω
Filter: Inductor (L_F) Resistor (R_F)	1 mH 1 Ω
DC-Side Capacitance (C_{DC})	1200 μF
Reference Voltage ($V_{DC, ref}$)	400 V
Power Converter	6-MOSFETs/diodes

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