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Effect of Various Parameters on Threshold Voltage of Virtually Fabricated Lightly Doped PMOS Device

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Abstract

This paper emphasis on the design, fabrication and analysis of 45 nm P type MOSFET device using SILVACO TCAD tool. The analysis was based on variation of various parameters like oxide thickness, threshold implant and halo implant (pockets) to analyze the threshold voltage. The drain versus gate and drain versus gate plots are being plotted using tony-plot. It has been observed that as the thickness of the oxide increases, threshold voltage also increases. Various other parameters like on current, off current, On/Off current ratio and DIBL has also been calculated for different oxide thicknesses. From the simulation results, the optimum threshold voltage of -0.026 V has been achieved.

Keywords: *MOSFET, SILVACO, threshold voltage, DIBL, Athena*

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INTRODUCTION

Bulk device has been the dominant device structure for integrated circuit design during the past decades, due to its excellent scalability. It is expected that such a device type will continue toward the 10 nm regime. To efficiently predict the characteristics of future bulk complementary metal oxide semiconductor (CMOS), the scaling trends of primary model parameters, such as the threshold voltage and gate dielectric thickness, need to be identified; their association in determining major device characteristics should be well included for accurate model projection. The parameters are varied slightly step by step and the effect on threshold voltage is observed using the SILVACO TCAD tool. In future scope of Integrated Circuits (ICs), there may be millions of transistors on a small piece of silicon. Naturally the fabrication and design of these IC's cannot be done without computer aids. Both the fabrication and design of these IC's require Electronic Design Automation tools (EDA). There is a need for highly precise software tools to analyze, simulation of the design and fabrication of integrated circuits. Lots of research has been done and still going on these issues. As a result we have got highly useful tools for design and fabrication of IC's [1].

DESIGN AND SIMULATION

A 45 nm PMOS bulk device has been designed having substrate doping 5e15 cm^{-3} with orientation <100> and with gate oxide thickness 1nm. Virtual fabrication of PMOS is done with ATHENA at 45 nm technology. The device has been designed in ATHENA of SILVACO software having specifications given in Table 1 below:

Table 1: *Specifications to Design 45nm PMOS.*

PROCESS	**PMOS DEVICE**
Initial Substrate Doping	Phosphorus=5e15 cm^{-3} Orientation=<100>
N-well Implant	Phosphorus=1.0x10^{12} cm^{-2}, Energy=100 KeV
Gate Oxide Growth	1 nm
Vt Implant	Arsenic = 2 e12, Energy=1 KeV
Poly-silicon Thickness	80 nm
LDD Implant	Boron=1.6e14, Energy=1 KeV
Pocket Implant	Arsenic= 4e13 cm^{-2} Energy=20 KeV
Source Drain Implant	Boron=1.6e15 cm^{-2} Energy=3 KeV
Final Rapid Thermal (RTA)	800°C/1 sec

SIMULATION RESULTS OF 45 NM PMOS

A PMOS device has been designed in ATHENA and simulated in ATLAS. The fabricated structure has been obtained in Figure 1 below which shows the various layers of conductor, insulator and semiconductor and also absolute net doping is shown in the structure. The result of process simulator developed from ATHENA was used as the input for a device simulator SILVACO Tool ATLAS and device characteristics can be examined. This provides an easy way of studying the effects of process parameter on device performance and both device structure and fabrication process can thus be optimized [2].

After the structure has been designed, then it is simulated to obtain the drain current versus gate voltage characteristics that can be seen and analysed in the graph shown below.

The Figure 2 shows I_D-V_{GS} curve at different drain voltages. It shows the variation of drain current with respect to gate voltages at different drain voltages. As the gate voltage is increasing the drain current increases linearly and after attaining a maximum value it saturates. The I_D-V_{GS} characteristics have been observed at different drain voltages at $V_{DS=}$ 0.05V and $V_{DS=}$ 1.2V to attain a clear understanding of the drain current versus gate voltage characteristics.

The Figure 3 shows I_D-V_{DS} curve at different gate voltages. As the drain voltage is increased, the drain current also shows a rise for different gate voltages. After drain voltage has increased to a certain value, both drain voltage and drain current attain a maximum value and don't increase beyond that. This can be observed in the graph shown [3].

After simulation various parameters of the PMOS are observed including gate oxide thickness, ON current, OFF current, DIBL and threshold. These parameters play a major role in determining the behaviour of the PMOS device, for instance the threshold voltage can be increased or decreased by varying the gate oxide thickness. The Table 2 shows the values of different parameters for PMOS GAUSS as below:

Table 2: *Extracted Results After Simulation.*

PARAMETERS	PMOS GAUSS
Gate Oxide Thickness, tox	1 nm
Threshold Voltage, Vtsat	0.26 V
Ion	811.13 µA
Ioff	9.34 nA
Ion/Ioff	86761.1
DIBL	0.07574

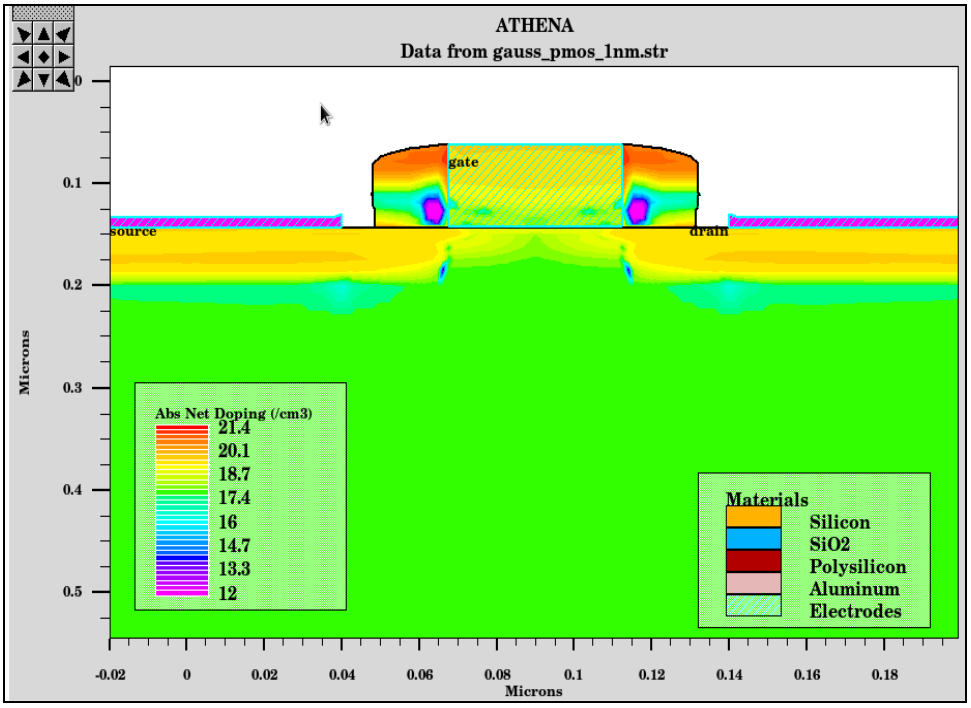

Fig. 1: *Structure of 45nm PMOS in Athena.*

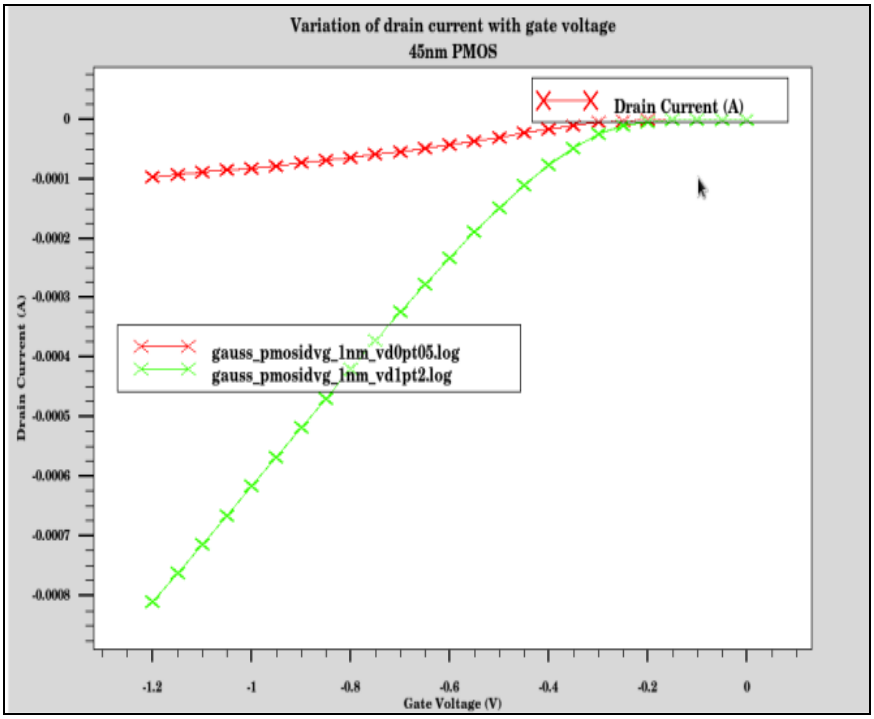

Fig. 2: *I_D-V_{GS} Curve at Different Drain Voltages.*

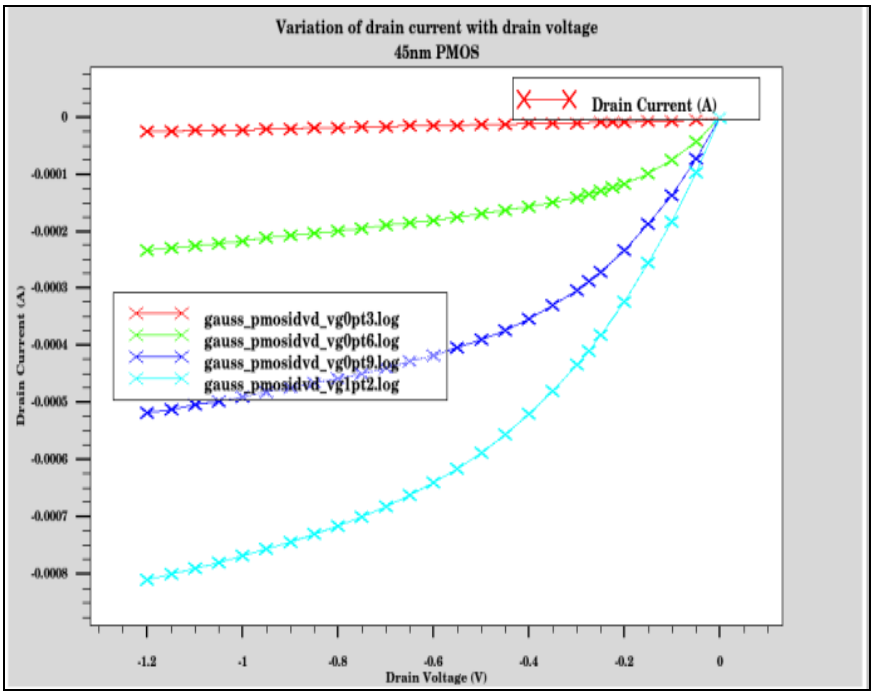

Fig. 3: *I_D-V_{DS} Curve at Various Gate Voltages.*

RESULTS AND DISCUSSIONS

Using the simulation tool on lightly doped PMOS device, the effect of various parameters such as oxide thickness, Vth adjust implant doping concentration, halo implant doping concentration are observed on parameters like DIBL, ON current, OFF current and threshold voltage [4].

Effect of Oxide Thickness on Threshold Voltage

The Table 3 gives us the relation between the different values of gate oxide thickness and the threshold voltages. With increase in thickness of gate oxide an increase in threshold voltage is observed. The gate oxide thickness is initially taken to be 0.001 μm and is increased

up to 0.002 µm. With this moderate increase in gate oxide thickness the threshold voltage is seen to be increasing by quite a good value.

The Figure 4 shows the graph between threshold voltage versus gate oxide thickness. As the thickness of gate oxide is increased, the threshold voltage is also increased [5].

Effect of V_{th} Adjust Implant Doping Concentration

The relation between Vt implant and threshold voltage is shown in Table 4 as given below:

It can be observed in the table obive that with an increase in Vt implant, threshold voltage also keeps on increasing without showing any irregularity or a dip in the graph.

The Figure 5 shows the relationship between the threshold voltage and the Vt implant. Vt implant values are placed on the horizontal axis, threshold voltage is placed on the vertical axis and a graph is plotted between the two to get a graphical idea of the increasing nature of threshold voltage with an increase in Vt implant. As we are increasing Vt implant voltage then the threshold voltage is increasing linearly.

Table 3: *Gate Oxide Thickness Variations.*

Gate Oxide Thickness	Threshold Voltage (V)
0.001 µm	0.264 V
0.0015 µm	0.400 V
0.002 µm	0.553 V

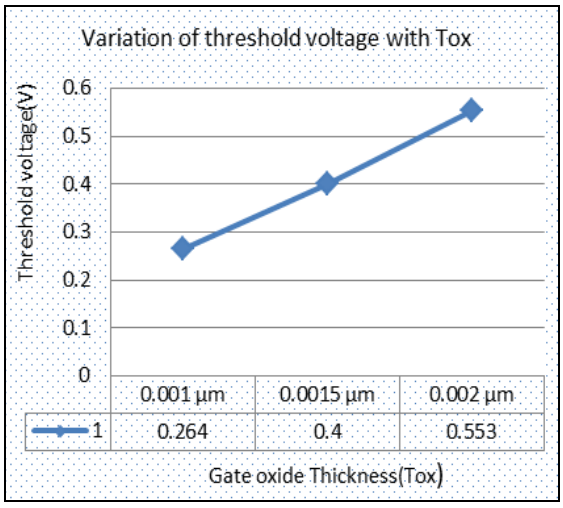

Fig. 4: *Threshold Voltages at Different Gate Oxide Thickness.*

Effect of Halo Implant Doping Concentration

The Table 5 gives us the relation between halo implant and threshold voltage, that is, with increase in halo implant an increase in threshold voltage is observed. The practical results as observed on SILVACO can be seen in the shown Table 5.

The Figure 6 shows the relation between the threshold voltage and halo implant. Halo implant concentrations are placed on the horizontal axis while the threshold voltages are placed on the vertical axis. As the concentration of halo implant is increasing the threshold voltage is increased [6].

Table 4: *Vt Adjust Implant Variation.*

Vt implant	Threshold voltage
1.5e12	0.246 V
2e12	0.264 V
2.5e12	0.287 V
3e12	0.309 V

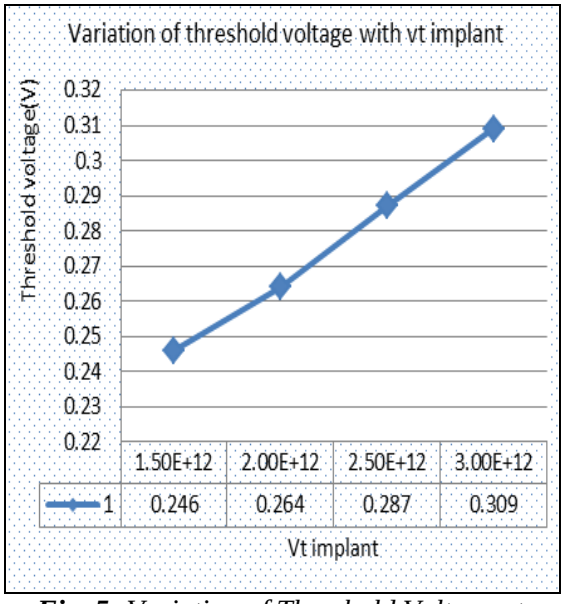

Fig. 5: *Variation of Threshold Voltage at Different Vt Adjust Implantation.*

Table 5: *Halo Implant Variations.*

Halo Implant	Threshold Voltage
3e13	0.214 V
4e13	0.264 V
5e13	0.316 V
6e13	0.370 V

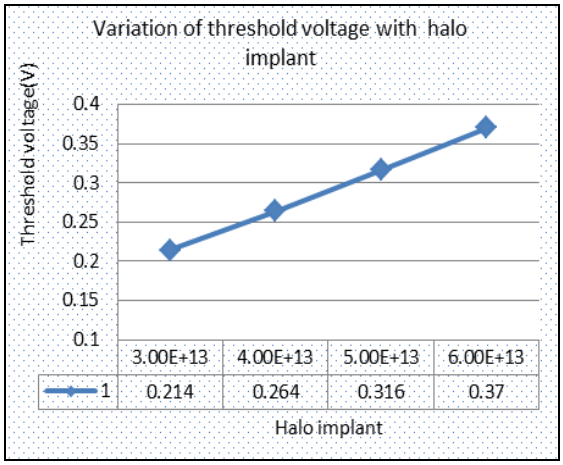

Fig. 6: *Variation of Threshold Voltage at Different Halo Implant Concentrations.*

Effect of Threshold Voltage Implant on ON Current and OFF Current

The ON and OFF currents are observed by varying the Vt implant. It can be concluded that with increase in Vt implant, ON current and OFF current both show a decrease in their values (Table 6).

Table 6: *Effect of Vt Implant on Current and OFF Current.*

Vt implant	ON Current	OFF current
1.5e12	8484 µA	18.88 nA
2e12	8111 µA	9.349 nA
2.5e12	7750 µA	4.725 nA
3e12	7401 µA	2.452 nA

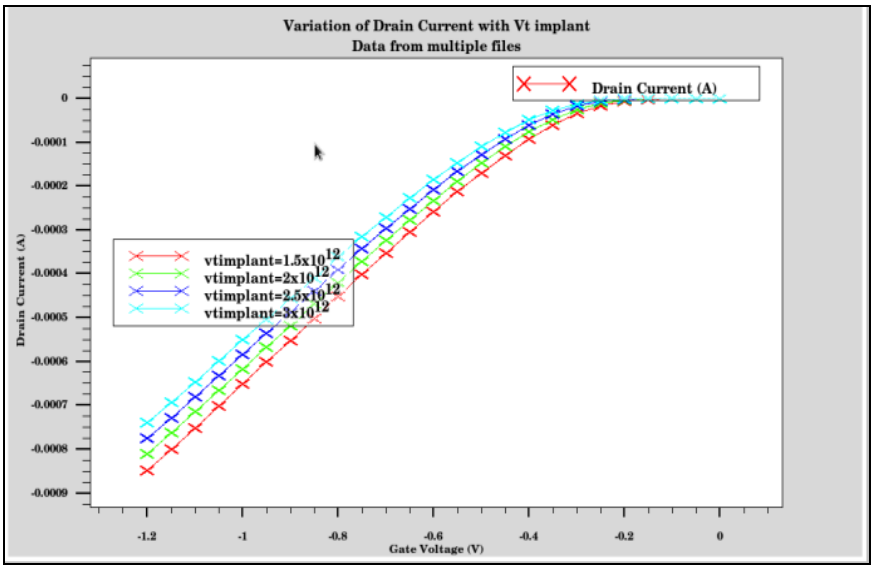

Fig. 7: *Variation of Drain Current with Vt Implant Data from Multiple Files.*

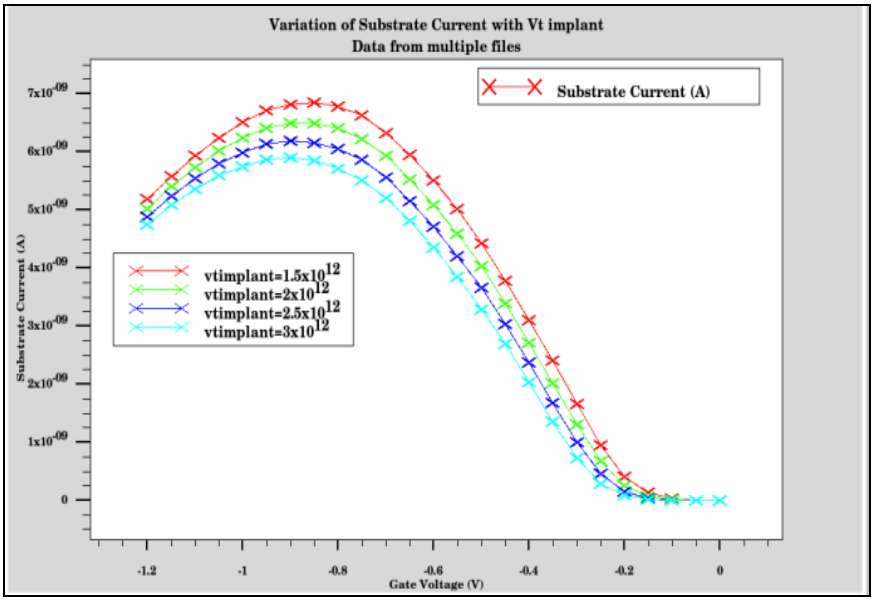

Fig. 8: *Variation of Substrate Current with Vt Implant Data from Multiple Files.*

Figure 7 shows the characteristic graph of drain current vs gate voltage, where gate current is placed on the vertical axis and the gate voltage is placed on the horizontal axis. The graphical representation of all the curves from multiple files shows an increasing nature, with a higher slope for lower values. These curves are seen to reach a saturation point after certain increase in the gate voltage and thus the slope of the curve is seen to be decreasing slowly until saturation. Figure 8 shown below plots a graph between substrate current vs gate voltage via data from multiple files. The different curves represent the behaviour for different values of Vt implant concentrations. The graph that attains the maximum substrate current is for the minimum Vt implant concentrations, while one that achieves minimum substrate current among the considered cases belong to the maximum Vt implant concentration [7].

It can be observed from the graph that with increase in Gate voltage the substrate current initially increases with an increasing slope, then the slope of the curve starts decreasing and it attains maxima. After attaining the maximum possible value for Substrate concentration, the curve now begins to decline with increase in gate voltage, i.e. after attaining the maxima a negative slope is observed. After increasing Gate voltage to a certain limit all the curves of different Vt concentrations attain saturation, that is, substrate concentration reach a value of 0 before the gate voltage reaches 0.

Effect of Halo Implant on ON Current and OFF Current

The SILVACO software is used to vary the halo implant concentrations and then observe its effects on ON current and OFF current. With increase in halo implant concentration ON current and OFF current both are seen to be decreasing. ON current is measured in a scale of micro metres while the OFF current is measured in a scale of nano metres (Table 7).

Figure 9 shown below is a plot between Drain current along vertical axis and gate voltage along the horizontal axis. Different plots represent different halo implant concentrations. Irrespective of halo implant concentrations, after certain value of Gate voltage the curves are seen to reach a saturation level beyond which no further increase in drain current is observed.

Table 7: *Effect of Halo Implant on ON Current and OFF Current.*

Halo Implant	ON Current	OFF current
3e13	9103µA	56.22nA
4e13	8111µA	9.349nA
5e13	7195µA	1.581nA
6e13	6340µA	0.258nA

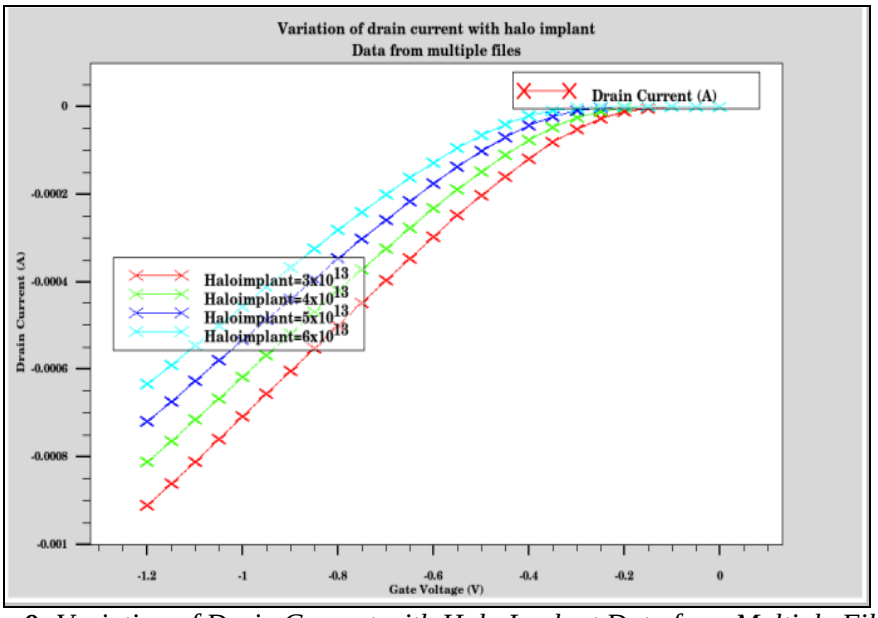

Fig. 9: *Variation of Drain Current with Halo Implant Data from Multiple Files.*

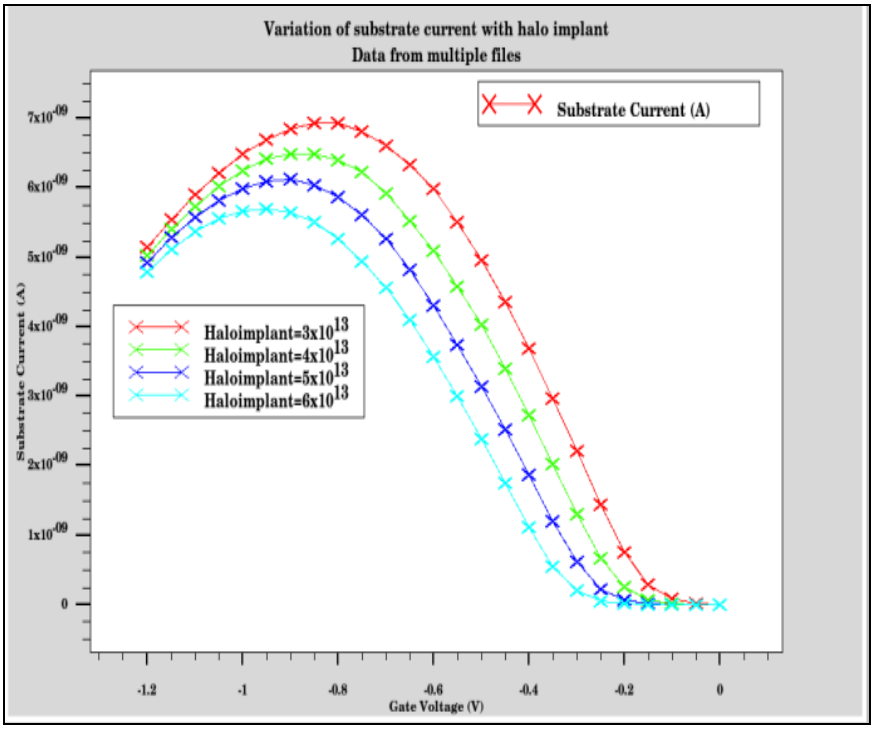

Fig. 10: *Variation of Substrate Current with Halo Implant.*

It has been observed that for greater value of halo implant concentration and a particular gate voltage below the saturation point, the value of drain current is lower. The below plot in Figure 10 shows that for a particular gate voltage before the saturation point, the greater is the halo implant concentration, greater is the substrate current. The curve initially has a positive slope which keeps on decreasing until maxima is reached, after attaining the maximum value of substrate current the curve attains negative slope and decreases until it reaches 0 substrate current [8].

Effect of Vt implant, Halo Implant and Tox on DIBL

When the small channel length MOSFETs are not scaled properly and the source/drain junctions are too deep or the channel doping is too low, there can be unintended electrostatic interactions between the source and the drain known as drain induced barrier lowering (DIBL). This leads to punch-through leakage or breakdown between the source and the drain, and loss of gate control. The result is a different curve of ID-VG after different value of drain voltage with respect to the source is applied. The simulation will use the structure file created from the previous Athena simulation.

Table 8: *Effect of Tox, Vt Adjust and Halo Implant on DIBL.*

Tox	Vt implant	Halo implant	DIBL
1 nm	2e12	4e13	0.07574
1.5 nm	2e12	4e13	0.111704
2 nm	2e12	4e13	0.141089
1 nm	1.5e12	4e13	0.077307
1 nm	2e12	4e13	0.07574
1 nm	2.5e12	4e13	0.072918
1 nm	3e12	4e13	0.071846
1 nm	2e12	3e13	0.079274
1 nm	2e12	4e13	0.07574
1 nm	2e12	5e13	0.07272
1 nm	2e12	6e13	0.06943

The values of Tox, Vt implant concentration and halo implant concentration are varied and the effects are observed on DIBL in Table 8 above. As Tox is increased the value of DIBL is also increased, along with that, with decrease in Halo implant concentration a decrease in DIBL is observed. Thus we can say that Tox and Halo implant concentration are directly proportional, while it is observed that with increase in Vt DIBL is decreased. Thus inverse proportionality is observed between Vt implant and DIBL.

CONCLUSION

The PMOS device has been designed using Gaussian doping profile and the variation of halo implant, gate oxide thickness and threshold implant affects the threshold voltage, drain current, leakage current and substrate current of the device. The estimated threshold voltage is -0.264 V and 9.349 nA leakage current is achieved for 45 nm PMOS device which is in line with international technology roadmap for semiconductor (ITRS) guideline. The purpose of this paper is to design a PMOS with channel length of 45 nm has been achieved. These techniques have shown good results in preventing the varying of the threshold voltage. The accuracy of the design can be determined from the output characteristics of the device simulation.

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