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Implementation of DCC Technique Using Differential Amplifier Based Filter in 90 nm CMOS Technology

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Abstract

Analog technique with feedback loop is applied to correct the duty cycle of any circuit without using more power. Pulse width modification is used to vary the duty cycle of clock signal. PMC cell is designed for expansion and contraction of pulse width. Differential amplifier based filter is used to detect the duty cycle of the particular clock signal. Differential amplifier and OpAmp are used to achieve adequate gain. The simulation is done in tanner EDA version_13 tool by using standard 90 nm technology. The schematic layout design of proposed DCC architecture is created in S-Edit. The system works at the frequency range of about 1 to 5 MHz.

Keywords*: Pulse width modification, duty cycle, delay locked loop, noise, sensitivity, EDA, tanner tool, SAR,PMC, CMFB*

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INTRODUCTION

The clock duty cycle is defined as the ratio of the output time during which the clock pulse is at a high level to the total clock cycle time period.

Duty Cycle = Thigh/Tperiod (1)

The duty cycle can be expressed as a ratio or as a percentage. Suppose a disk drive operates for 1 sec, then is shut off for 99 sec, then is run for 1 sec again, and so on. The drive runs for one out of 100 sec, or 1/100 of the time, and its duty cycle is therefore 1/100, or 1%.

Commonly used phase-locked loop (PLL) and CDR circuits often use multiple stages to facilitate a stable and consistent operation [1, 2]. Phase locked loops and delay-locked loops achieve high-accuracy clocks with low phase noise, but do not ensure a 50% duty cycle for the output waveform. Broadly there are two approaches, that are: 1) analog, with feedback loops and 2) digital, with and without the use of feedback. In the study by Mu and Svensson, an analog pulse width control loop is used with a ring oscillator to generate a reference signal [3]. In the study by Chen *et al.*, the analog duty-cycle correction (DCC) uses a current-starving technique to shrink or stretch pulses [4]. An analog loop with a digitally controlled charge pump was used by Cheng *et al.* [5].

Digital feedback techniques include the use of a binary search algorithm with SAR [6], time to digital converters [7, 8] and phase-alignment [9].

A duty cycle is the fraction of one period in which a signal or system is active. Duty cycle is commonly expressed as a percentage or a ratio. Duty cycle is the proportion of time during which a component, device, or system is operated.

PMC CONCEPT

The PMC is used to vary the linear pulse width with control voltage. As shown in Figure 1, it is essentially an inverter, whose drive strength is modified by variable current sources connected to the output node [1]. As a result, the rise and fall times of the signal are increased or decreased, as necessary. This slew-deformed waveform is rectified by a comparator whose trip-point is close to the mid-rail voltage.

PROPOSED WORK

This method of duty cycle measurement and correction consists of six-transistor PMC,

Differential Amplifier based filter and differential amplifier.

The complete circuit schematic is shown in Figure 2 [10]. Multiple units of the PMC are cascaded. The common mode voltages VCM1 and VCM2 are locally generated on chip. When there is a change in the duty cycle at the input, it is carried through by the PMCs and the DCD produces a differential error voltage proportional to the change in the duty cycle. This is amplified by the DA, which also generates a differential control voltage around the bias that is required for the PMCs. The control voltage moves in opposing directions for the complementary paths. When the duty cycle increases in the positive input path, there is a corresponding decrease in the complementary path. When the control voltage reduces the duty cycle in the positive path, it simultaneously increases the same in the complementary path. This leads to a differential DCC.

PMC Cell

Figure 3 shows the actual implementation of the PMC. When the rise or fall times are increased by reducing the drive strength, the pulse width is contracted by the comparator. Conversely, when the rise or fall times are shortened, there is pulse width expansion. The last inverter stage acts as the comparator.

Duty Cycle Detector

The DCD produces a differential analog output corresponding to the input duty cycle as shown in Figure 4. It is analogous to a charge pump used in most PLLs. In this implementation, the DCD is a DA-based filter. The pole is placed well below the lowest frequency of operation of the loop. The input signals are integrated with the average value of the signal being proportional to the duty cycle.

Differential Amplifier followed by OpAmp

A DA is used to provide gain in the feedback loop and also to bias the differential control voltages around a locally generated bias value. The primary sources of error are the offset of the amplifier and the mismatches between the differential halves.

Figure 5 shows the schematic of differential amplifier. A single output, which is proportional to the difference between two inputs, is needed very often. Thus, we need to combine the two outputs.

This is achieved using current mirror loads. The basic single ended differential amplifiers play a very important role. Hence, we started designing of single ended differential amplifier by replacing source resistance by improved current sources.

The differential amplifier with active load and single ended output is the commonly used differential amplifier in CMOS analog circuits. This single ended differential amplifier has excellent features in terms of self-bias capability, common mode rejection, voltage gain and the gain-bandwidth product.

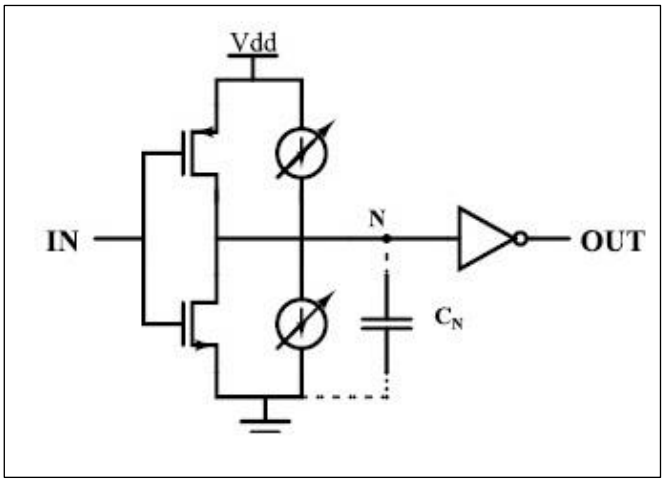

Fig. 1. *Conceptual Diagram of PMC.*

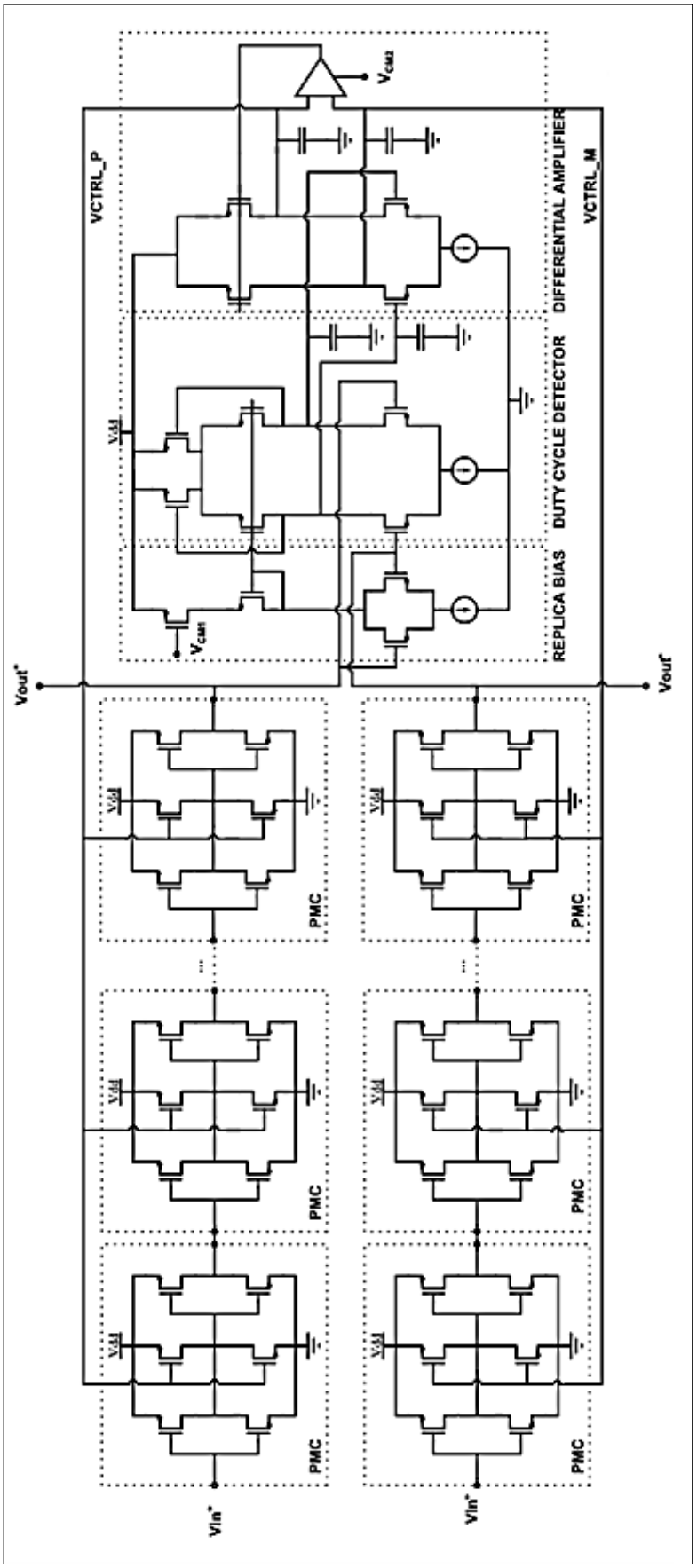

Fig. 2. *Architecture of DCC.*

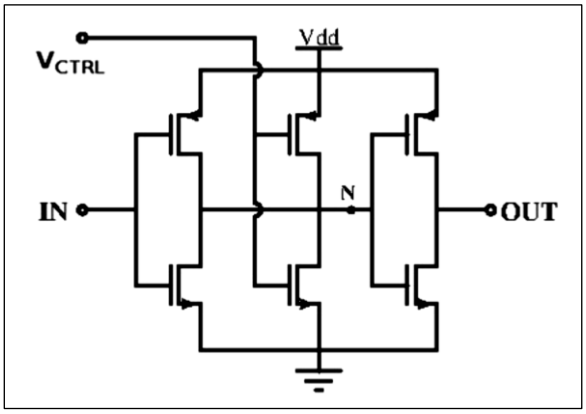

Fig. 3. *Schematic of the PMC.*

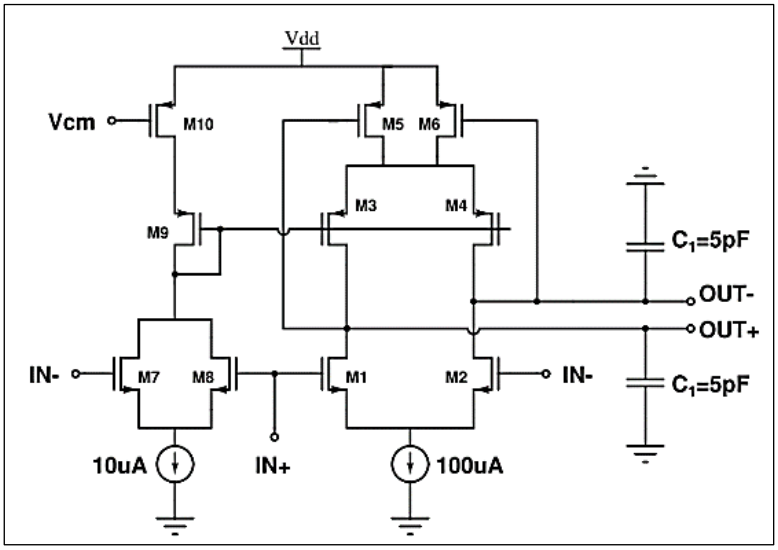

Fig. 4. *Schematic of DCD.*

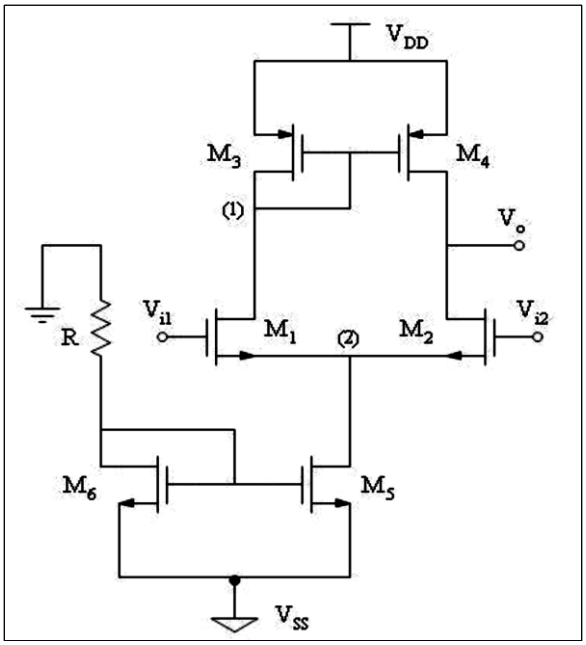

Fig. 5. *Schematic of Differential Amplifier.*

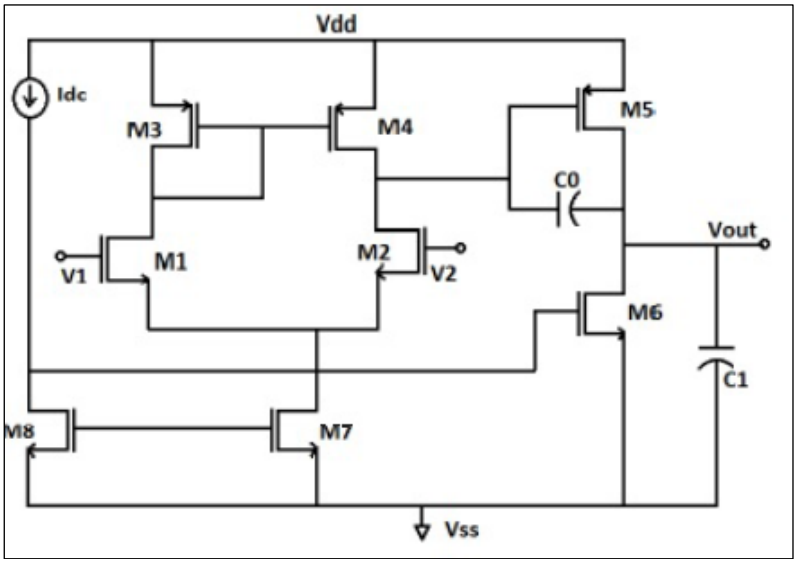

Fig. 6. *Schematic of OpAmp.*

OpAamp has two stages, as shown in Figure 6 where stage-1 is the differential amplifier and common source amplifier becomes stage-2. The differential amplifier has two different voltage inputs vin+ and vin- which amplify the differences between two input voltages. Since the gain obtained from the first stage is not sufficient, it uses common source amplifier at second stage. Thus, the output of this differential amplifier continues to enter the common source amplifier where gain is increased further. In order to obtain low gain at high frequencies and maintain the device stability, it includes compensation circuit whenever the device is in negative feedback condition.

Amplifiers are devices which take a relatively weak signal as an input and produce a much stronger signal as an output. The operational amplifier (or op-amp) is a special kind of amplifier used in equipment such as stereo equipment and medical cardiographs (which amplify the heart beat).

RESULTS AND DISCUSSION

The proposed design is simulated in Tanner tool.

PMC Cell

PMC comprises of six transistors as shown in Figure 7. It is essentially an inverter, whose drive strength is modified by variable current sources connected to the output node. This slew-deformed waveform is rectified by a comparator whose trip-point is close to the mid-rail voltage.

The output waveform of PMC is shown in Figure 8. The PMC is used to vary the linear pulse width with control voltage. As a result, the rise and fall times of the signal are increased or decreased, as necessary.

Duty Cycle Detector

The schematic of DCD is shown in Figure 9. Duty cycle detector consists of replica bias followed by differential amplifier based circuit. The output node has a large capacitor of 5pF on each differential arm. It is an active low-pass filter, which generates the differential dc average. The dc average is directly proportional to the duty cycle. MOS capacitors are used to minimize the area. A replica-based Common Mode Feedback (CMFB) and biasing arrangement can be seen on the left part of the circuit. The CMFB scheme exploits the replica structure to set the output common mode. Transistors used in replica bias are scaled versions of the transistors used in filter.

The output of DCD is totally dependent on Vdd and duty cycle of clock signal. So the output is directly proportional to the duty cycle of a particular clock signal. The output waveform is as shown in Figure 10.

Two inputs with opposite phase are applied to the DCD. So, the signal output (Vout= Vout2-Vout1) is directly proportional to the duty cycle of clock signal.

Differential Amplifier

The output of DCD is to be amplified from mV range to V range. So the differential amplifier is used to amplify the weak signal from DCD. The schematic of differential amplifier is shown in Figure 11. The basic single ended differential amplifiers play a very important role in analog circuits. Hence the design of single ended differential amplifier by replacing source resistance by improved current sources is achieved. The differential amplifier with active load and single ended output is the commonly used differential amplifier in CMOS analog circuits.

As shown in Figure 12, the output of differential amplifier is amplified. Vin1 and Vin2 are applied at the input side of differential amplifier. In the first clock cycle, Vin1 is 1 V and Vin2 is 0 V. So, the output is 5 V. Similarly, in the 2nd clock cycle, Vin1 is 0 V and Vin2 is 5 V, so the output is 0 V. Hence, the output of amplifier is directly proportional to the Vin1 with adequate gain. The input to the differential amplifier is about 0–1 V. And the output of the same is 0–5 V.

OpAmp

Figure 13 shows the schematic of two-stage OpAmp. Opamps are the most commonly used devices in electronic circuits. They are used in filters, differentiators, integrators, digital-analog convertors and comparators. The total gain of two-stage OpAmp is defined by Av. The corresponding gain is calculated as the product of Av1 and Av2. Av1 is called as differential amplifier gain and Av2 is called as common source amplifier gain. So, two-stage OpAmp is used when gain requirement is very high.

The design and optimization of two stages CMOS OPAMP has been done by using 90 nm technology in Tanner tool. Figure 14 shows the output waveform of OpAmp circuit.

Input to the OpAmp are two clock cycles named as Vin1 and Vin2. Vin1 and Vin2 are to be in opposite phase to each other. Vin1 varies from 0 to 5 V, whereas Vin2 varies from 5 to 0 V. Output clock signal shows that it follows Vin1 with adequate gain.

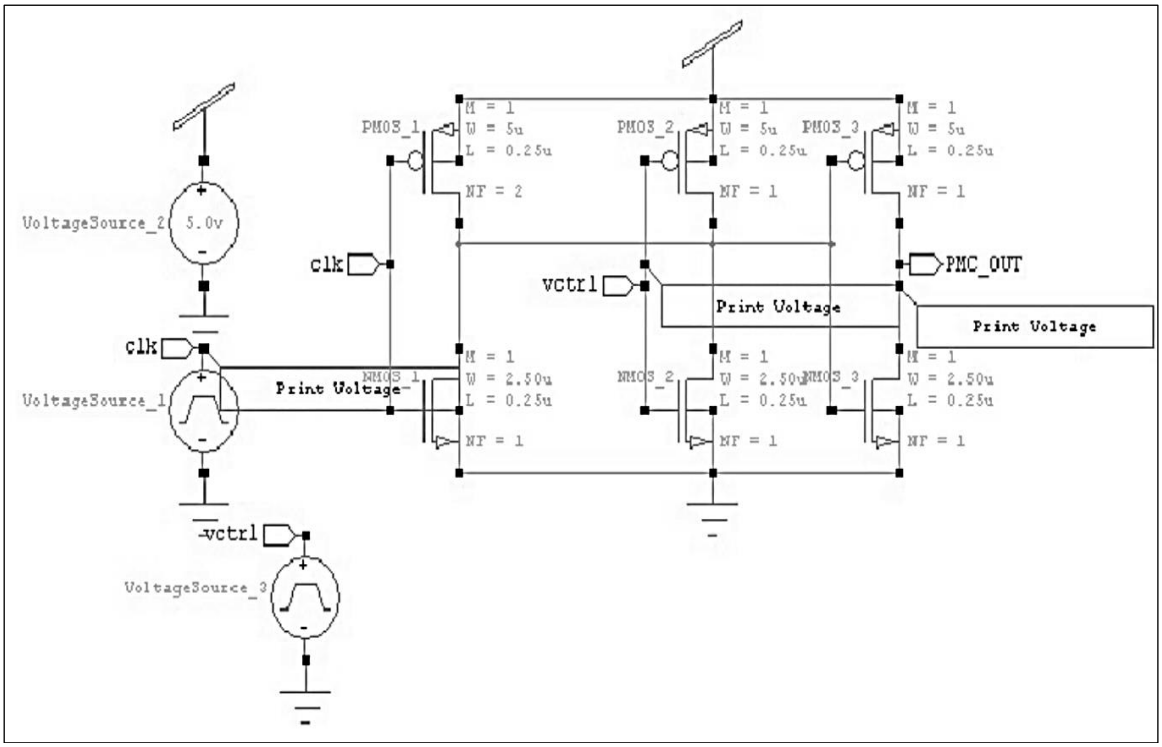

Fig. 7. *Schematic of PMC in Tanner Tool.*

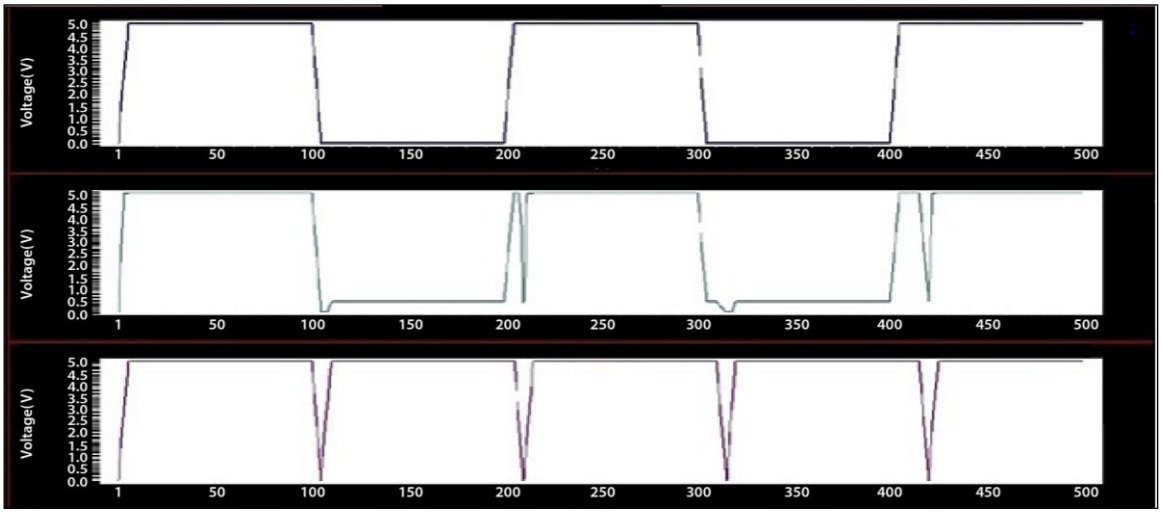

Fig. 8. *Waveform of PMC in Tanner Tool.*

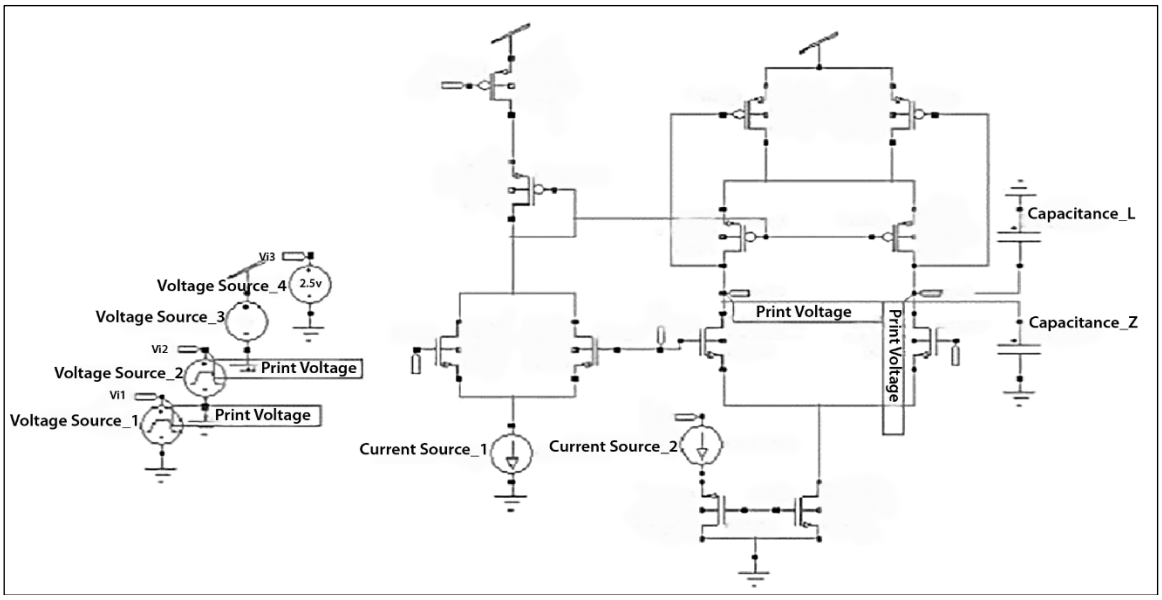

Fig. 9. *Schematic of DCD in Tanner Tool.*

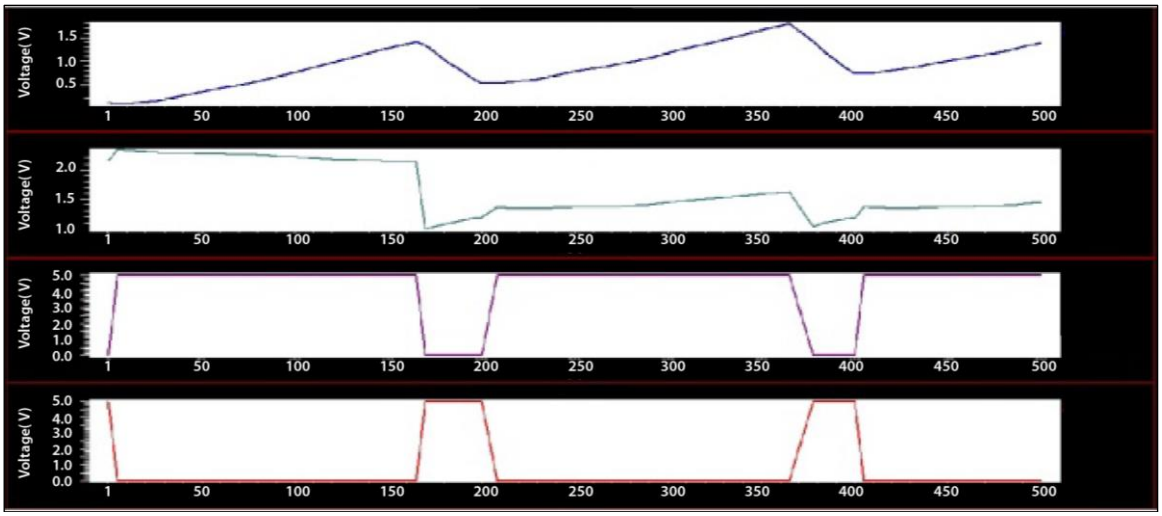

Fig. 10. *Waveform of DCD in Tanner Tool.*

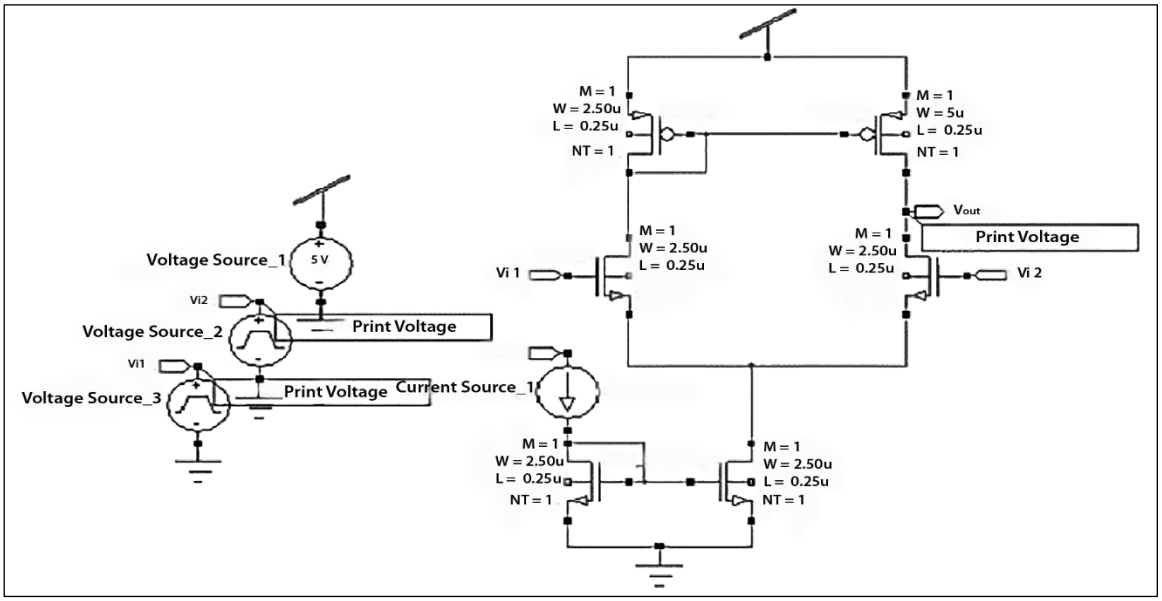

Fig. 11. *Schematic of DA in Tanner Tool.*

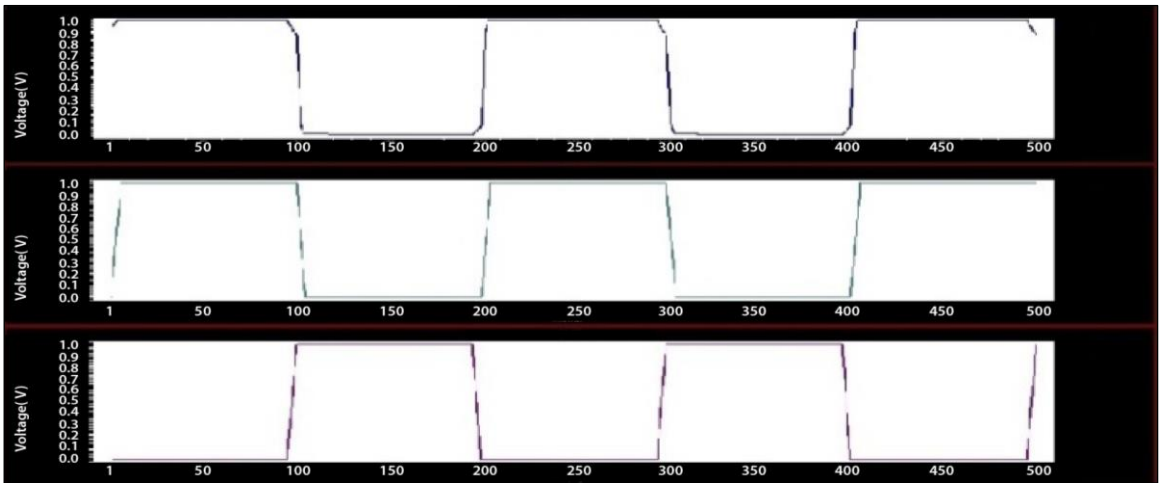

Fig. 12. *Waveform of DA in Tanner Tool.*

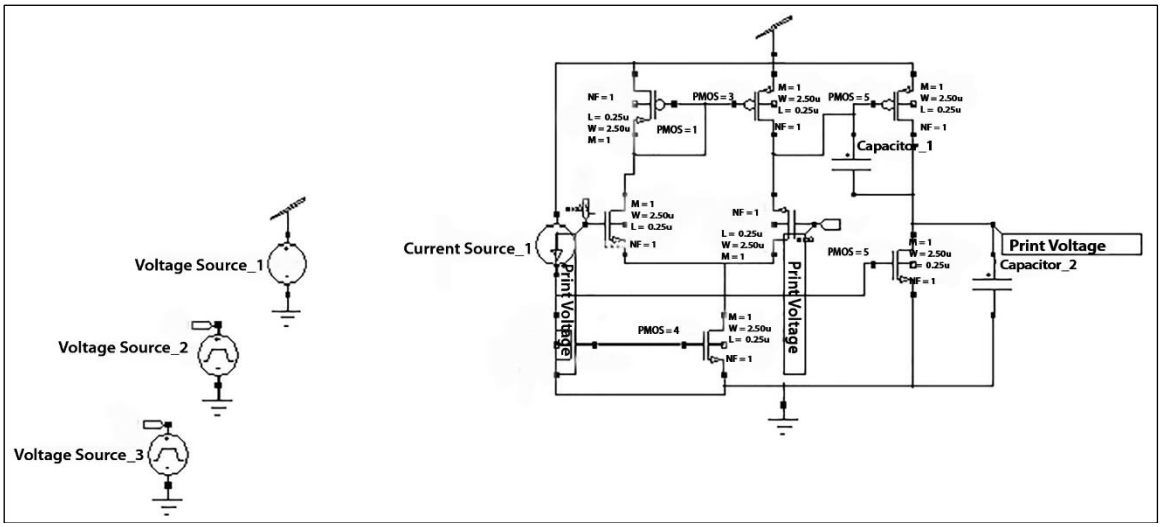

Fig. 13. *Schematic of OpAmp in Tanner Tool.*

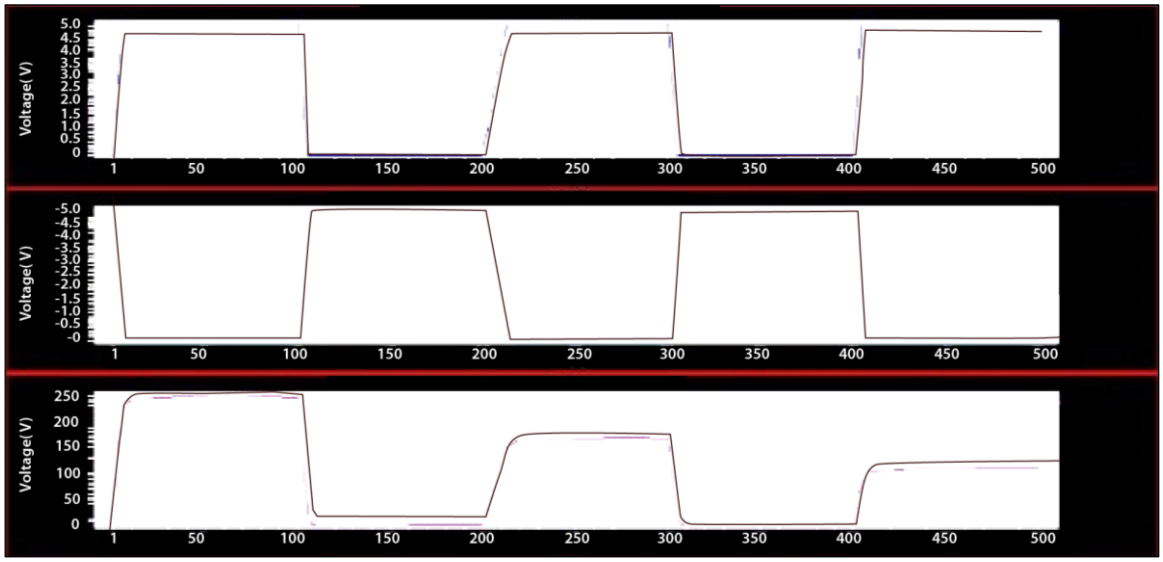

Fig. 14. *Waveform of OpAmp in Tanner Tool.*

CONCLUSION

The DCC circuit is fabricated in a 90 nm CMOS process. Since, the absolute time by which the pulse can be contracted or expanded is limited by the number of PMCs used in this implementation, it can be observed that the input duty-cycle range over which the correction can be performed, is limited at 5 MHz. Although the correction technique works at 5 MHz, the accuracy to which it can correct, is limited for larger duty-cycle errors. This can be addressed by adding more PMCs in the circuit. An input duty-cycle variation of 30% where 70% will be corrected to within 0.6% of the target duty cycle of 50%. It has been demonstrated that this analog feedback technique can perform well where digital techniques fail at the same technology node. Compared with other analog techniques, the proposed PMC with voltage control is proposed to perform well consuming 1.066 mW power. This system can be used and applicable in DDR, charge pump and PLL.

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