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Design of Energy Efficient Clock System

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Abstract

Energy efficiency is a key metric for energy constrained Ultra Low Power (ULP) VLSI applications such as wireless sensor nodes, pace makers, hearing aids etc. These applications need clock system in their signal processing and communication sub-system. Moreover, clock system plays a vital role in governing the reliability, power consumption and performance of synchronous system. In today's era of portable electronics, power consumption has emerged as a forefront design metrics. Sub-threshold operation of device is an excellent option to have the ULP system. However, degraded performance and exacerbated variability are the major concerns of sub-threshold circuits. This work investigates the performance of CMOS clock system and hybrid (combination of CMOS and DTMOS) clock system in sub-threshold regime. The results indicate that the proposed hybrid clock system exhibit better output frequency, SLP, PDP, EDP and robustness compared to CMOS clock system.

Keywords: *Sub threshold, Voltage Controlled Oscillator (VCO), Current Starved VCO (CSVCO), Clock Distribution Network (CDN), Power Delay product (PDP), Energy Delay product (EDP), Slew Latency Product (SLP), Monte Carlo simulation*

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INTRODUCTION

In today's era of miniaturization and portable electronics, elevating power density has emerged as a critical issue. In deep nanometer regime, the dual advantage of high speed and low power can no longer be yielded from technology scaling. Moreover, International Technology Roadmap for Semiconductors (ITRS) has predicted that in deep nano-regime, the expected high integration will encounter substantial difficulties, possibly preventing the continued improvements in figure of merit, such as low power and high performance [1]. Clock system is an inevitable part of synchronous system and vital component in many portable applications like wireless sensor nodes, pace makers, hearing aids etc. The power consumption is a primary concern for portable applications, since battery life is paramount in such applications. Since clock system is the most power hungry circuit, the design of ULP clock system will reduce the overall power consumption of a system and increase the battery life of the handheld applications.

Sub-threshold operating regime has great potential to satisfy the demand of ULP of hand-held applications [2]. However degraded performance and exacerbated variability are the stumbling blocks that restrict the wide applicability of sub-threshold circuits. Though power consumption is reduced by an order of magnitude in sub-threshold region, correspondingly the performance also gets degraded in this regime. The work in this study focuses on design of an energy efficient clock system.

Clock generator and Clock Distribution Network (CDN) together constitute a clock system. Output frequency, slew, skew and latency are important parameters of clock system. Researchers have explored various techniques to improve the performance parameters of the clock system. Tolbert *et al.* emphasized the significance of clock slew for reliability of sub-threshold circuits and devised a methodology to control clock slew while minimizing the energy [3]. However, clock skew was not considered in their work. Seok *et al.* focused on skew for buffered and un-

buffered tree. However, they did not take slew into consideration [4]. Seok *et al.* proclaimed that un-buffered tree minimizes the clock skew [4]. On the contrary, Zhao *et al.* concluded from their work that, buffered clock circuit is an important means to achieve the required clock slew and skew and they presented the variation-aware methodology that controls both clock skew and slew to maximize frequency and minimize clock power [5]. Jorgenson *et al*. reported a promising approach of solving the timing problems by using the clock-less asynchronous design [6]. However due to lack of computer-aided design (CAD) tools for the synthesis and optimization of asynchronous circuits, the implementation of the asynchronous systems faces many design difficulties [7]. The gate-drive voltage of CMOS transistors in pseudo-differential delay, cells were boosted through the use of quasi-floating gate (QFG) architecture by Kamalinejad *et al.* [8]. The boosted gate-drive voltages facilitate oscillation with supply voltages as low as 90mV which accordingly results in a low power consumption. Thus, the different parameters of clock system like frequency, slew, latency, energy efficiency are comprehensively investigated by very few researchers. This work presents a clock system with enhanced frequency, improved PDP, EDP, SLP and better robustness.

The rest of the paper is organized as follows: Next part describes the energy efficient clock generator circuit and focuses on the design of H tree CDN optimized for better slew. The simulation results are discussed afterwards, followed by conclusion.

ENERGY EFFICIENT CLOCK GENERATOR CIRCUIT

Voltage Controlled Oscillator (VCO) is generally used as a clock generator circuit in VLSI chips. The communication sub-systems in many applications demand the clock generator circuit with wide frequency range. CMOS based ring oscillator is an appropriate choice in today's era of hand held devices since CMOS oscillators are small in size, consume low power and have wide tuning range [9]. Current Starved VCO (CSVCO) is a CMOS based ring oscillator whose frequency is controlled by the control voltage.

Figure 1 shows the schematic of CMOS based CSVCO. In this circuit, MP1 and MN1, MP2 and MN2, MP3 and MN3, MP4 and MN4, MP5 and MN5 form CMOS inverters, while MN12-MN16 and MP12-MP16 operate as current sinks and sources respectively. The drain current of MN11 and MP11 is same and is set by the input control voltage. The currents in MN11 and MP11 are mirrored in each inverter/current source stage. Consequently the change in control voltage, $V_{control}$, induces a global change in the inverter current and acts directly on the speed.

The frequency of N stage CSVCO is expressed as [10]:

$$f_{oscillator} = \frac{I_d}{N*C_{Tot}*V_{DD}} \quad (1)$$

Where, I_d represents the driving current, C_{Tot} is the total capacitance and V_{DD} is the supply voltage.

The sub-threshold leakage current, given by Eq.(2), acts as the driving current in sub-threshold operation in bulk CMOS [10].

$$I_d = I_0 e^{\frac{(V_{GS}-V_{th})}{nV_t}} \quad (2)$$

Where, $I_0 = \mu C_{ox} \frac{W}{L} (n-1) V_t^2$

μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, V_t=(KT/q) is the thermal voltage, K is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge, V_{th} is the threshold voltage of the MOSFET and n is the sub-threshold slope factor.

In Weak Inversion (WI) operation, the drive current I_d is dominated by the diffusion current in contrast with conventional operation of CMOS circuit where drift current is dominant factor in contributing I_d. The poor drive current in sub-threshold region leads to degradation in performance of sub-threshold circuits. Dynamic Threshold MOS (DTMOS) logic is one of the techniques recommended by researchers to enhance the switching frequency [11]. In DTMOS logic, the body terminal of MOS device is connected to its gate. This enhances the performance when device is on. Figure 2 illustrates the NMOS and DTMOS device. Though the back gate biasing improves the drive current of the device, it also increases the capacitance of DTMOS device.

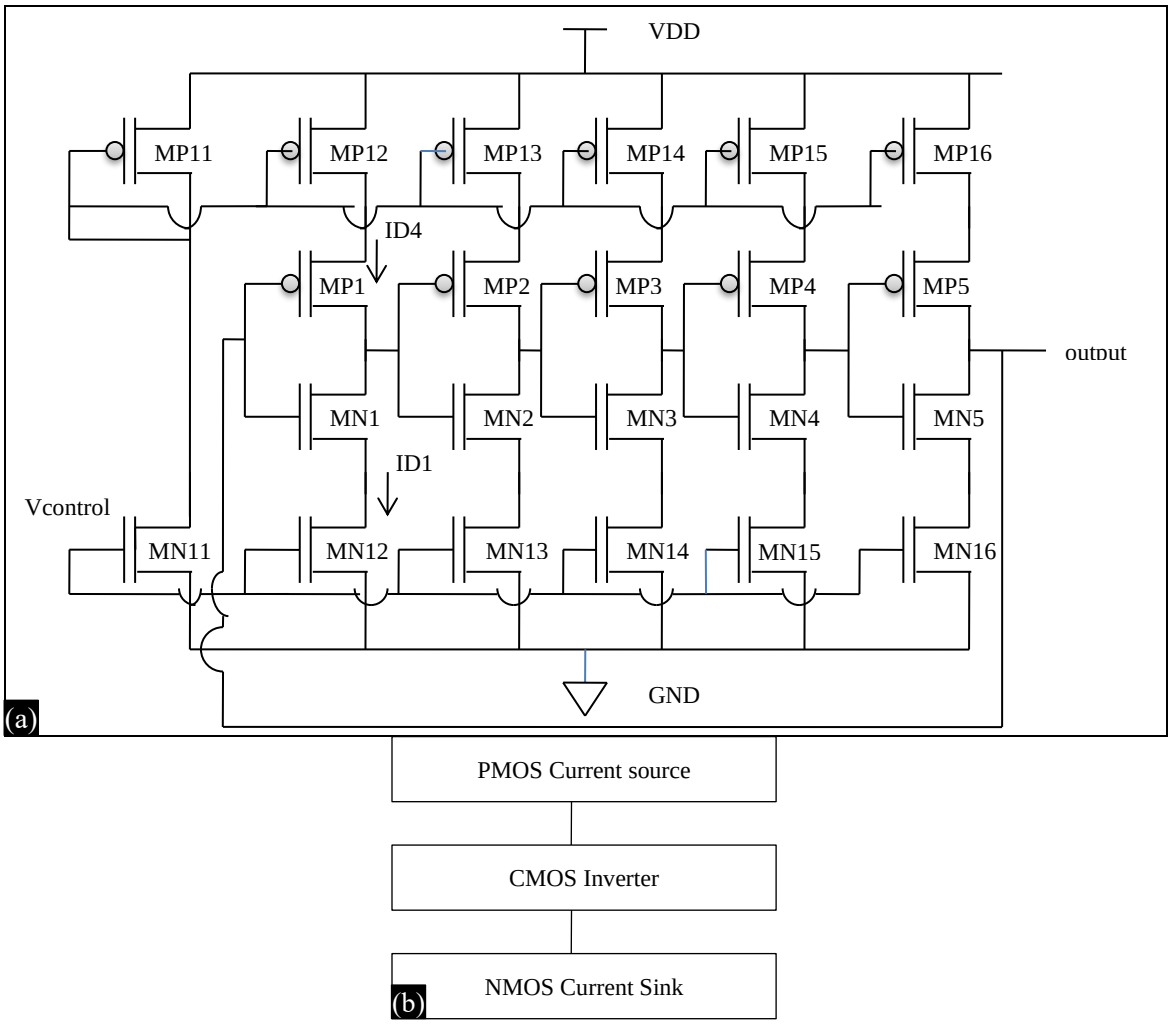

Fig. 1. *(a) Schematic of CMOS CSVCO, (b) Structure of CMOS CSVCO.*

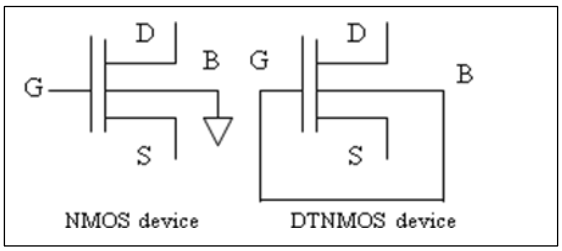

Fig. 2. *NMOS and DTNMOS Device.*

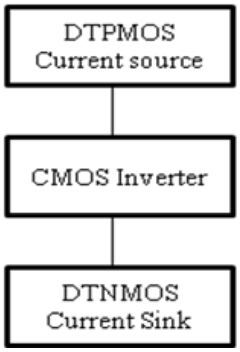

Fig. 3. *Structure of Hybrid CSVCO.*

The frequency of CSVCO is decided by the drive current and capacitance of inverter in ring oscillator as illustrated in Eq.(1). Therefore a hybrid CSVCO with DTMOS current source and sink; to improve the drive current and CMOS inverters; to have low capacitance will eventually improve the output frequency of VCO as concluded from our findings in Walunj *et al.* [12].

A five-stages CMOS CSVCO and hybrid CSVCO as illustrated in Figures 1 and 3 respectively are designed using HSPICE at 32nm technology node using PTM model and simulated at 0.3V supply and 0.2V control voltage to investigate their performance in sub-threshold regime [13]. Figure 4 illustrates the output frequency of CMOS CSVCO and hybrid CSVCO. As illustrated in Figure 4, the output frequency of hybrid CSVCO is

increased by 55% compared to CMOS CSVCO. But hybrid CSVCO gives this increase in output frequency at the expense of increase in power consumption. Power Delay Product (PDP) is a measure that gives energy efficiency of circuit. Figure 5 illustrates the PDP of the CMOS and hybrid CSVCO. The hybrid CSVCO shows better PDP by 22% compared to CMOS CSVCO.

Thus, the results indicate that the hybrid CSVCO is an energy efficient CSVCO compared to CMOS CSVCO and therefore an optimal choice for sub-threshold clock generator circuit.

H TREE CDN WITH DTMOS-CMOS BUFFERS AT SINK NODES

Clock Distribution Network (CDN) is the largest network and consumes larger power in a synchronous system. Researchers have recommended tapered H tree for lower skew and power consumption [14]. Conventionally, buffers are distributed throughout the CDN to improve the slew [15]. Insertion of buffers reduces the capacitance of this large network and hence improves the slew parameter. The suitability of conventional CDN for sub threshold regime was investigated in [16]. A strategy of having a uniform H tree with a pair of buffer only at sink nodes in CDN, as illustrated in Figure 6, was proposed by Walunj *et al.* [16]. The pair of buffer consists of CMOS buffer connected to sink node preceded by a DTMOS buffer. Clock system with CMOS CSVCO and H tree CDN depicted in Figure 6 was simulated and the results indicated that this clock system exhibited better slew with an added advantage of reduced power consumption compared to clock system having CMOS clock generator and conventional tapered H tree [16].

SIMULATION RESULTS

In this work, the simulation set up consists of clock generator whose output is fed to the D Flip Flops via H tree CDN with DTMOS-CMOS buffers at sink nodes as illustrated in Figure 7. Following two-clock systems are simulated:

1. Clock system in Figure 7 with CMOS CSVCO clock generator circuit-CMOS clock system.
2. Clock system in Figure 7 with hybrid CSVCO clock generator circuit-hybrid clock system.

The set up in Figure 7 is simulated with supply voltage of 0.3V and control voltage of 0.2V. The comparative performance of CMOS clock system and hybrid clock system is illustrated in Figure 8.

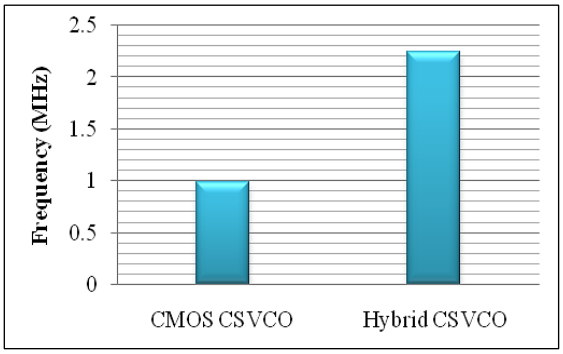

Fig. 4. *Output Frequency of CMOS CSVCO and Hybrid CSVCO.*

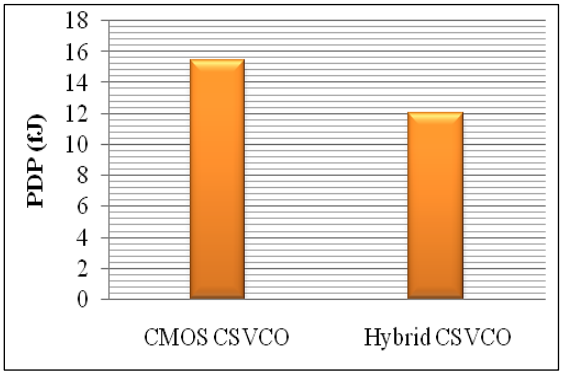

Fig. 5. *PDP of CMOS CSVCO and Hybrid CSVCO.*

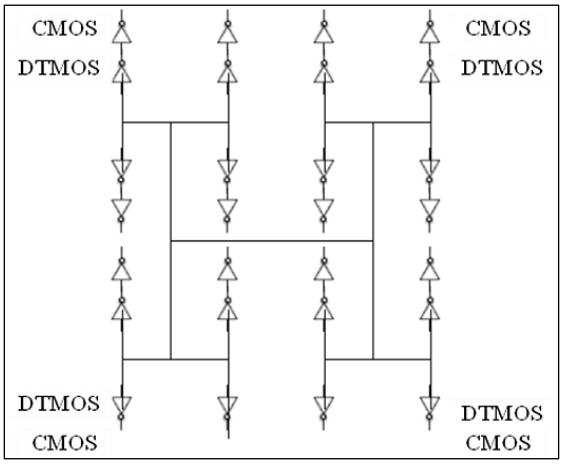

Fig. 6. *H-Tree CDN with DTMOS-CMOS Buffers at Sink Nodes.*

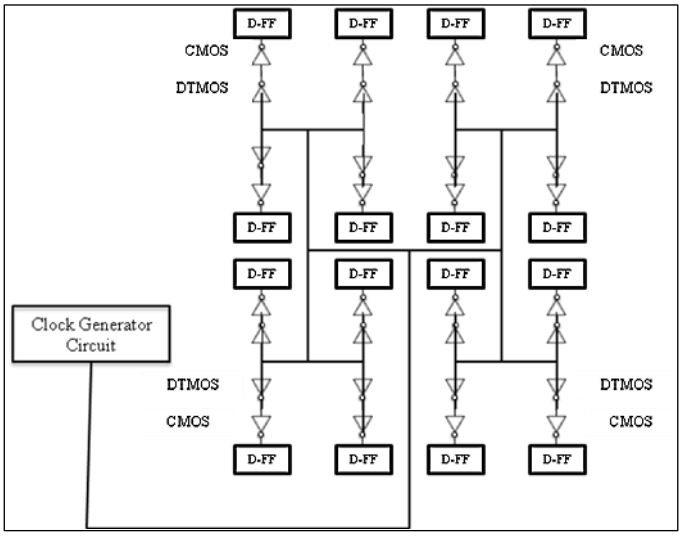

Fig. 7. *Simultion Set-Up of Clock System.*

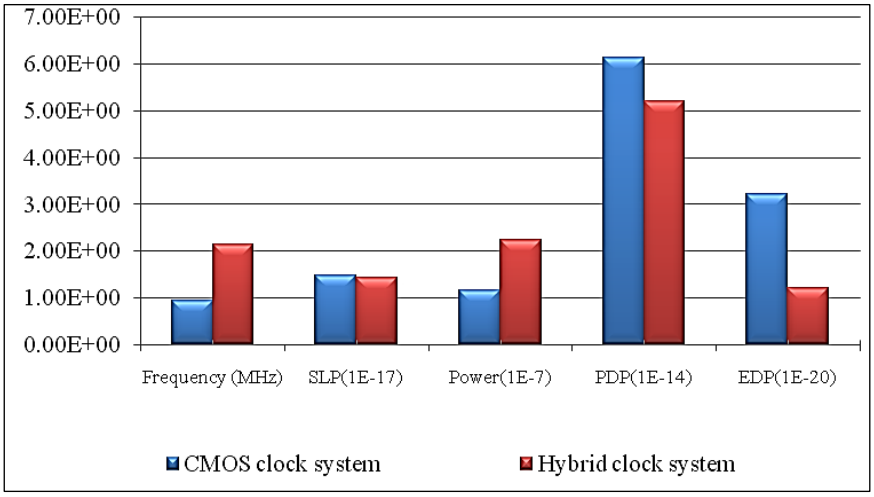

Fig. 8. *Performance Comparison of CMOS and Hybrid Clock System.*

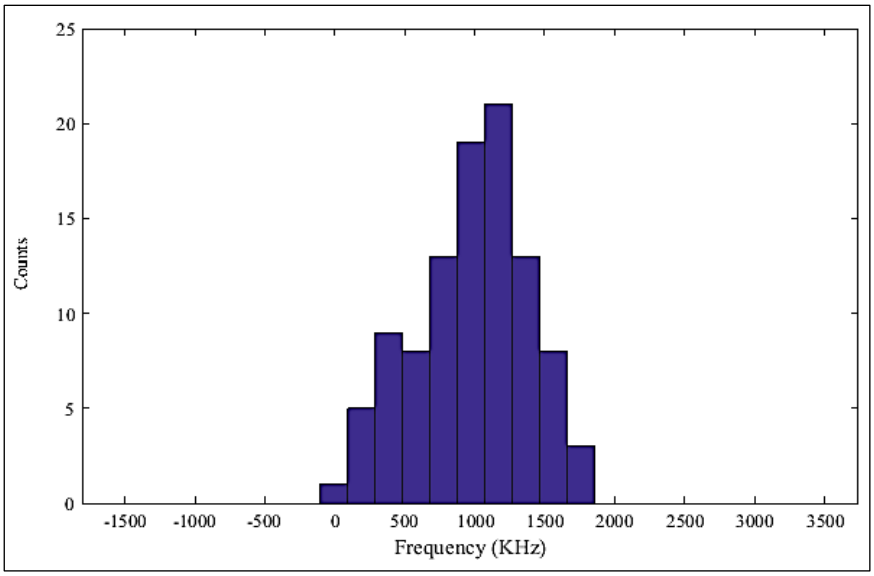

Fig. 9. *Impact of PVT Variation on Output Frequency of CMOS Clock System.*

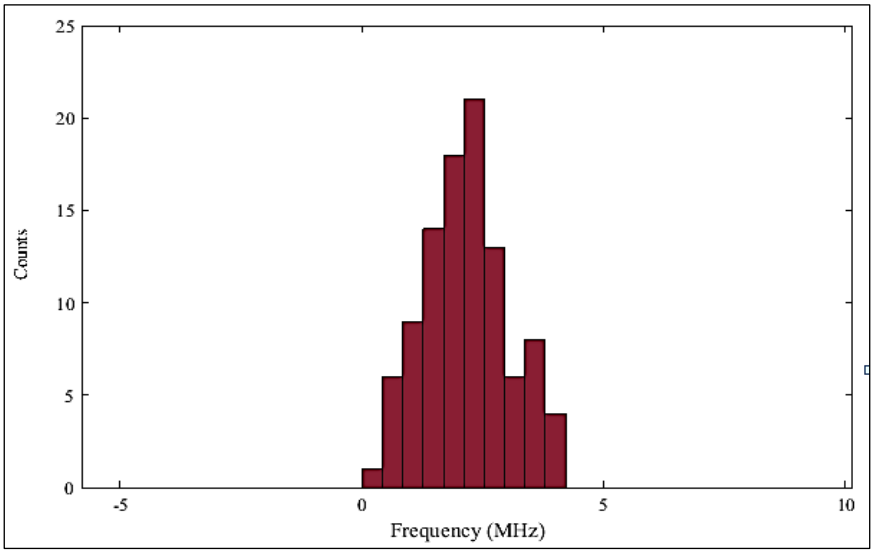

Fig. 10. *Impact of PVT Variation on Output Frequency of Hybrid Clock System.*

The sub-threshold clock system with conventional buffered CDN exhibit better slew whereas sub-threshold clock system with un-buffered CDN exhibit better latency [17]. For better performance, both slew and latency must be minimized. In order to investigate the performance of the CMOS and hybrid clock system in Figure 7, a new performance parameter, SLP-(Slew Latency Product) is coined in this work. For better performance, SLP must be less. As indicated by Figure 8, hybrid clock system exhibits higher frequency by 55% and lower SLP by 4% compared to CMOS clock system. Though the increase in performance of hybrid clock system comes at the cost of increase in power consumption, the PDP and EDP exhibited by hybrid clock system are better compared to CMOS clock system by 15.3 and 62.4% respectively. Thus hybrid clock system proves to be energy efficient compared to CMOS clock system.

In order to investigate the robustness of CMOS and hybrid clock system against Process, Voltage and Temperature (PVT) variation, Monte Carlo simulations are performed considering 10% variation in threshold voltages, 10% variation in supply voltage and 20% variation in temperature. The results of variation in frequency of CMOS and hybrid clock system are depicted in Figures 9 and 10 respectively. The CMOS clock system exhibits 4.4% increased variation in frequency compared to hybrid clock system.

CONCLUSION

The energy efficient sub-threshold clock system has been successfully designed at 32nm technology node. This study explored the hybrid clock system and CMOS clock system for output frequency, SLP, PDP and EDP parameters. The sensitivities of the two-clock system against PVT variations are also explored in this work. It has been found that the hybrid clock system exhibits better robustness against PVT variation besides having higher output frequency, low SLP, PDP and EDP and therefore is a good choice for sub-threshold clock system.

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