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An Explicit Approach to Compare Crosstalk Noise and Delay in VLSI RLC Interconnect Modeled with Skin Effect with Step and Ramp Input

Shilpi Lavania[1]*, *Sunil Kumar Sharma*[2]
[1]Hindustan College of Science & Technology, Farah, Mathura, India
[2]Moti Lal Nehru National Institute of Technology, Allahabad, India

ABSTRACT

As the technology is acquiring frequency of the Giga-hertz range noise and delay calculations and avoidance of such factors in VLSI interconnects have become dominant to be considered. This paper represents a comparison between the crosstalk noise voltage level measured when the RLC on-chip interconnect was modeled when the skin effect was considered under step input and the crosstalk voltage measured when the RLC line was modeled with skin effect under ramp input. In this paper, we have proposed a detailed discussion about the relevance of the input applied to any interconnect that can affect the whole system integrity. The importance and dominance of the skin effect cannot be ignored. But apart from the high frequency effect like skin effect and proximity effect, it is also very important to observe that these factors may harm the system integrity if the wrong input is applied. This paper reflects the approximated noise and delay variations in different cases of inputs applied to the Global RLC interconnect.

Keywords: *VLSI, RLC, interconnect, crosstalk, delay calculation*

****Author for Correspondence*** Email: shilpi.lavania@gmail.com, rockstardking20@gmail.com
Tel:+91-9528996841

INTRODUCTION

With the development of ultra large scale integrated circuit (IC) process, interconnect delay is playing the dominant role as compared to the gate delay. Simple but effective analytical delay models of interconnects are useful for IC designers to avoid the timing issue problem and to optimize the design, such as minimizing delay [1–5]. Hence, it is necessary to build accurate and effective delay estimation models for interconnects. The amount of interconnect among the devices tends to grow super linearly with the transistor counts, and the chip area is often limited by the physical interconnect area. Several factors bound to the technology contribute to the increase of crosstalk problems like the increase of the number of metal layers [6], the increase of the line thickness, the density of integration and the reduction of the spacing between lines. This set of new challenges is referred to as signal integrity in general and raises issue for the system integrity. Crosstalk typically happens between two adjacent wires when their cross coupling capacitance is sufficiently large to influence each other’s electrical characteristic. Especially for an on-chip bus crosstalk, noise is a serious problem for VLSI design. In bus structure, crosstalk immunity is more important because long interconnect wires often run together and in parallel. Interconnect lines may be coupled to study the effects of mutual inductive and capacitive coupling, such as crosstalk. both a distributed and a lumped model for these macro models [7]. In this paper, we have made efforts to justify that not just the high frequency effect can affect the system integrity and response but also the applied input to these interconnects along with such high frequency effects, i.e., proximity effect and skin effect can make situation worse when the system is very sensitive and higher degree of performance is required .The rest of the paper is organized as follows: Section 2 discusses the basic theory, transmission line model, and crosstalk. Section 3 describes the comparison of the responses under both the iputs. Section 4 shows the experimental and simulation results. Finally, Section 5 concludes the paper.

BASIC THEORY

Continuous advances in integrated circuit (IC) technology have resulted in smaller device dimensions, larger chip sizes, and increased complexity. There is an increasing demand for circuits with higher speeds and higher component densities. In recent years, growth of GaAs on silicon (Si) substrate has met with a great deal of interest because of its potential application in new hybrid technologies. GaAs-on-Si unites the high-speed and optoelectronic capability of GaAs circuits with the low material cost and superior mechanical properties of the Si substrate. The heat sinking of such devices is better since the thermal conductivity of Si is three times more than that of GaAs. This technology is expanding rapidly from research to device and circuit development. So far, various IC technologies have employed metallic interconnections, and there is a possibility of using optical interconnections in the near future. Of late, the possibility of using superconducting interconnections is also being explored [8]. A transmission line [9] can be described at the circuit level using series or parallel inductance and resistance combined with capacitance.

The skin effect can be represented at the circuit level as a combination of frequency-dependent resistance and inductance. However, frequency-dependent circuit elements are not suitable for time-domain analysis. Therefore, a circuit representation based on frequency-independent elements is desirable [10]. The “skin effect” is the tendency of high-frequency current to concentrate near the outer edge, or surface, of a conductor, instead of flowing uniformly over the entire cross-sectional area of the conductor. The higher the frequency, the greater the tendency for this effect to occur. There are three possible reasons we might care about skin effect. The resistance of a conductor is inversely proportional to the cross-sectional area of the conductor. If the cross-sectional area decreases, the resistance goes up. The skin effect causes the effective cross-sectional area to decrease. Therefore, the skin effect causes the effective resistance of the conductor to increase. The skin effect is a function of frequency. Therefore, the skin effect causes the resistance of a conductor to become a function of frequency (instead of being constant for all frequencies). This, in turn, impacts the impedance of the conductor. If we are concerned about controlled impedance traces and transmission line considerations, the skin effect causes trace termination techniques to become much more complicated. If the skin effect causes the effective cross-sectional area of a trace to decrease and its resistance to increase, then the trace will heat faster and to a higher temperature at higher frequencies for the same level of current [11].

CROSSTALK

Crosstalk is defined as the energy imparted to a transmission line due to signals in adjacent lines. Crosstalk magnitude is a function of rise time, signal line geometry and net configuration (type of terminations, etc.). A common method of shielding is to place ground or power lines at the sides of a victim signal line to reduce noise and delay uncertainty [12]. The crosstalk between two coupled interconnects is often neglected when a shield is inserted, significantly underestimating the coupling noise. The crosstalk noise between two shielded interconnects can produce a peak noise of 15% of VDD in a 0.18 µm CMOS technology [13]. An accurate estimate of the peak noise for shielded interconnects is therefore necessary. In the complicated multilayered interconnect system, signal coupling and delay strongly affect circuit performances. Thus, accurate interconnect characterization and modeling are essential for today’s VLSI circuit design. Two major impacts of crosstalk are: (i) crosstalk induced delays, which change the signal propagation time, and thus may lead to setup or hold time failures; (ii) crosstalk glitches, which may cause voltage spikes on wire, resulting in false logic behavior. Crosstalk affects mutual inductance as well as inter-wire capacitance. When the connectors in high-speed digital designs are considered, the mutual inductance plays a predominant role compared to the inter-wire capacitance. The effect of mutual inductance is significant in deep submicron (DSM) technology since the spacing between two adjacent bus lines is very small. The mutual inductance induces a current from the aggressor line onto a victim line which causes crosstalk between the parallel lines. This in turn alters the performance parameters of on-chip VLSI interconnect system.

In multi-conductor systems, crosstalk can cause two detrimental effects: first, crosstalk will change the performance of the transmission lines in a bus by modifying the effective characteristic impedance and propagation velocity. Second, crosstalk will induce noise onto other lines, which may further degrade the signal integrity and reduce noise margins[14].

CROSSTALK AND DELAY MODELING WITH SKIN EFFECT

This section deals with the crosstalk and delay variations with respect to the high frequency effect phenomenon called the “skin effect.” The skin effect is the tendency of high frequency current density to be highest at the surface of a conductor and then to decay exponentially toward the centre [11].

The possible reasons for the skin effect are the following:
The resistance of a conductor is inversely proportional to the cross-sectional area of the conductor. If the cross-sectional area decreases, the resistance goes up. The skin effect causes the effective cross-sectional area to decrease. Therefore, the skin effect causes the effective resistance of the conductor to increase [15].

The skin effect is a function of frequency. Therefore, the skin effect causes the resistance of a conductor to become the function of frequency. This, in turn, affects the impedance of the conductor. The inductance decreases as the frequency increases [16].

PROPOSED WORK

We first consider the interconnect system consisting of a coupled RLC line where the inductance and capacitive coupling is not considered:

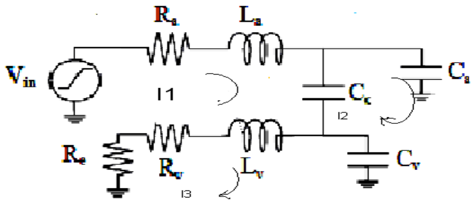

Fig. 1 RLC Transmission Line.

This section is again divided into two parts. The first part presents the crosstalk noise and delay response of the above RLC interconnect when the step input is applied. The second section deals with the crosstalk and delay response when the ramp input is applied to the same interconnect line.

Table I RLC Parameters for a Minimum-Sized Wire in a 0.18 µM Technology.

Parameter(s)	Value/m
Resistance (R)	120 kΩ/m
Inductance (L)	270 nH/m
Capacitance (C)	240 pF/m
Coupling Capacitance (C_c)	682.49 fF/m

Section(a)
This section consists of the delay and crosstalk response of the transmission line as shown in Figure 1 when the step input is applied**.**

The crosstalk simulation for this circuit with skin effect is given as [10]. Figures 2 and 3 show the crosstalk noise at the output node without and with skin effect respectively. Figures 4 and 5 are the delay responses of the same transmission line with and without skin effect respectively.

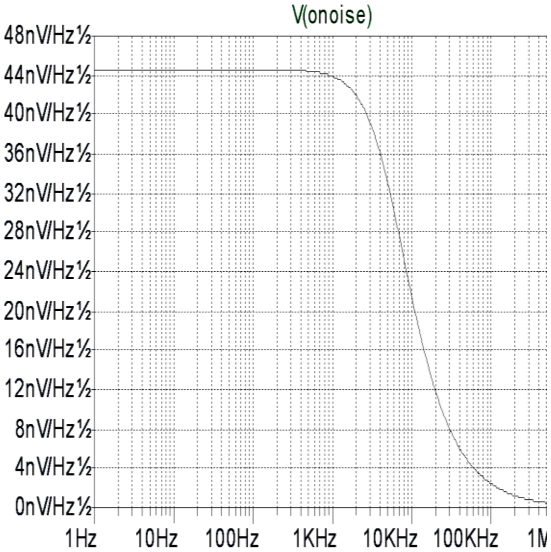

Fig. 2 Output Crosstalk Node Noise without Skin Effect under Step Input

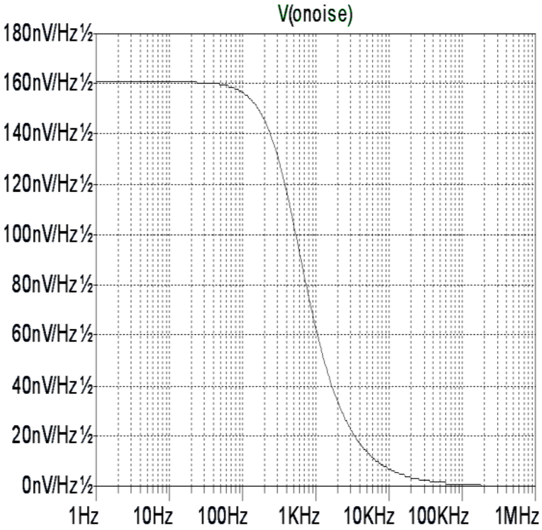

Fig. 3 Output Node Crosstalk Noise under Skin Effect under Step Input.

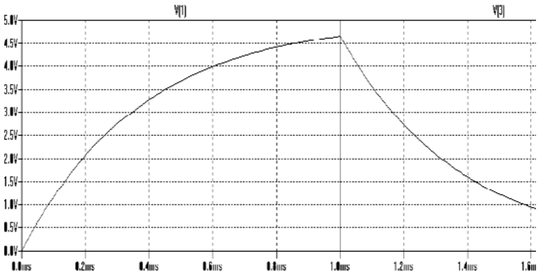

Fig. 4 Delay with Skin Effect under Step Input.

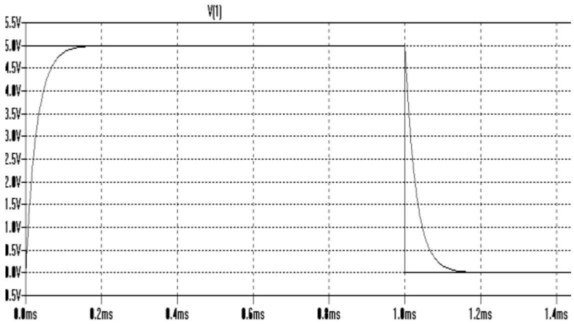

Fig. 5 Delay without Skin Effect under Step Input.

Table I Experimental Result under Step Input without Skin Effect.

Ex	**R_s (KΩ)**	**C_L (fF)**	**SPICE Delay (ms)**	**Proposed Model Delay (ms)**
1	1	10	0.1023	0.1041
2	5	50	0.1124	0.1147
3	10	750	0.1393	0.1491
4	50	1000	0.1679	0.1779
5	100	1500	0.19595	0.1986

Table II Experimental Result Under Input with Skin Effect.

Ex	**R_s (KΩ)**	**C_L (fF)**	**Spice Delay (ms)**	**Proposed Model Delay (ms)**
1	1	10	0.1893	0.1904
2	5	50	0.4524	0.5167
3	10	750	0.7993	0.8191
4	50	1000	0.8699	0.8879
5	100	1500	0.9595	0.9986

Section (b)

This section consists of the delay and crosstalk response of the transmission line as shown in

Figure 1 when the ramp input is applied.The crosstalk simulation for this circuit with skin effect is given as [10]. Figures 6 and 7 show the crosstalk noise at the output node without and with skin effect respectively. Figures 8 and 9 are the delay responses of the same transmission line with and without skin effect respectively:

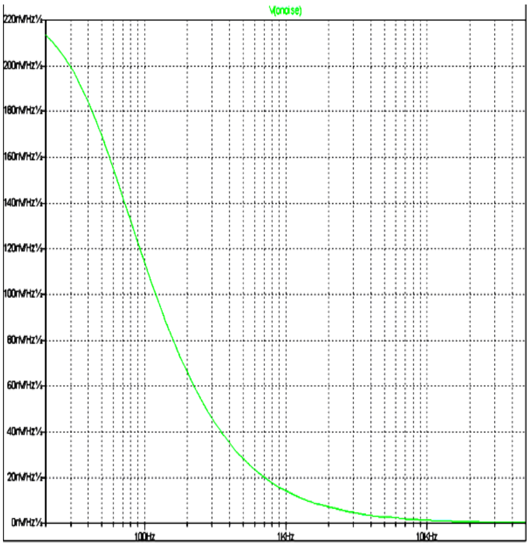

Fig. 6 Output Node Crosstalk Noise without Skin Effect under Ramp Input.

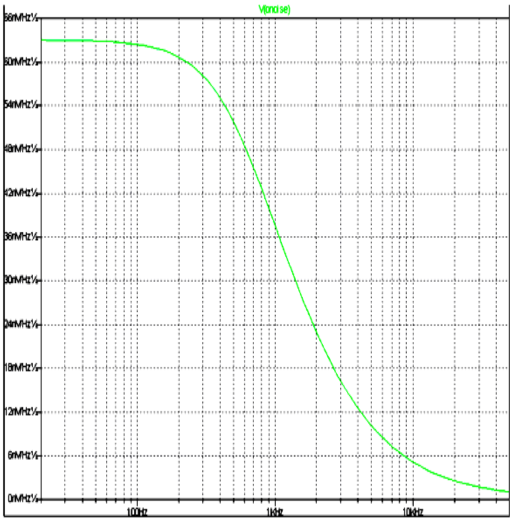

Fig. 7 Output Node Crosstalk Noise with Skin Effect under Ramp Input.

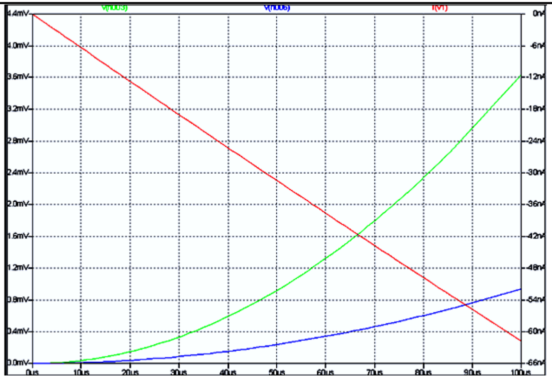

Fig. 8 Delay with Skin Effect under Ramp Input.

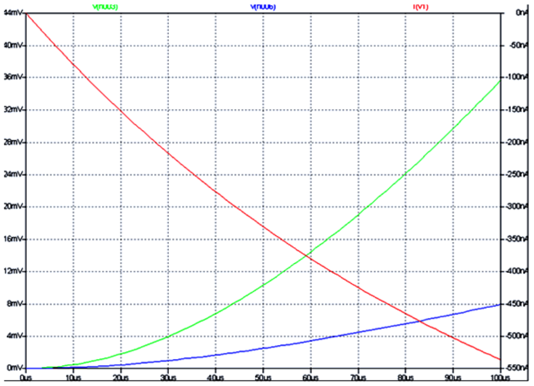

Fig. 9 Delay without Skin Effect under Ramp Input.

Table III Experimental Result under RAMP Input without Skin Effect.

Ex	R_s (KΩ)	C_L (fF)	Spice Delay (ms)	Proposed Model Delay (ms)
1	1	10	0.1123	0.1152
2	5	50	0.1198	0.1171
3	10	750	0.1479	0.1474
4	50	1000	0.1779	0.1881
5	100	1500	0.1995	0.1994

Table IV Experimental Result under RAMP Input with Skin Effect.

Ex	R_s (KΩ)	C_L (fF)	Spice Delay (ms)	Proposed Model Delay (ms)
1	1	10	0.1739	0.1921
2	5	50	0.358	0.6437
3	10	750	0.7739	0.8129
4	50	1000	0.8475	0.8942
5	100	1500	0.9757	0.9976

CONCLUSIONS

In this paper, we have discussed the problem of crosstalk noises and delay in high-speed coupled interconnect systems.

This paper provides relevance of the applied input in RLC interconnect where one of the dominant high-frequency effect, i.e., skin effect has been considered. In this paper, we have proposed an idea that if the various high-frequency effects are affecting the system and even in the worst case the bad result can be achieved if a great precaution is applied in applying the input. Wrong input can affect the system and signal integrity as a whole.

In section (a) when the step input is applied, delay and crosstalk noise are observed. Table I and Table II represent the data collected, whereas in section (b) when the ramp input is applied again the delay and the crosstalk noise are observed. But the delay has been increased in case of the ramp input. The simulation results justify the proposed theory and idea. Hence, this paper has proposed a detailed relevance of the applied input nature on the performance of the system.

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