Journal of VLSI Design Tools & Technology
Volume 1, Issue 1-3 Compilation 2011

STM JOURNALS

Analysis of VLSI Circuits Designed with Single and Dual Channel Strained Silicon MOSFETs in Nanoregime

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ABSTRACT

In this paper, performance of the VLSI circuits designed with strained silicon MOSFETs is analysed and compared with bulk MOSFET. Emphasis is being given on the evaluation of speed, power and noise characteristics. An inverter circuit designed with single channel and dual channel biaxial strained MOSFETs of 40 nm channel length and 0.3 germanium mole-fraction is being taken to evaluate the performance through simulation. The device design and circuit simulation is done in Sentaurus TCAD tool. The designed strained silicon MOSFETs shows increased carrier mobility, carrier velocity and drive current than bulk MOSFET. Dual channel biaxial strained MOSFET shows even much better performance than single channel biaxial strained MOSFET. The inverter circuit designed with this dual channel biaxial strained silicon MOSFETs shows much lesser delay and power consumption as compared to circuit designed with single channel strained MOSFET and bulk MOSFETs. Thus, the circuits designed with strained silicon MOSFETs are preferred in digital applications for low power and high speed circuits.

Keywords: *Biaxial single channel strained MOSFET, Biaxial dual channel strained MOSFET, Carrier mobility, Carrier velocity, Compressive strain, Delay, Inverter, Noise Margin, Tensile strain*

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INTRODUCTION

Over many years device dimensions are reducing day by day. In this trend of scaling, supply voltage scaling is adopted to improve the performance of the circuits [1]. The requirements of digital circuits to be used in modern-day VLSI applications are low power consumption, high noise tolerance and high speed. Though supply voltage scaling reduces the power consumption but it also increases the delay and reduces the noise tolerance of the device [2]. Therefore, supply voltage scaling cannot be considered as a viable option to improve the overall performance of the digital circuits. In the present technology, strained silicon MOSFETs has emerged as the most preferred option to improve the performance of the device. This is because strained silicon MOSFETs increases the carrier mobility which in overall improves the performance of the device and moreover, its fabrication is compatible with existing fabrication technology. The impact of mechanical strain on the electron and hole mobility is being studied from many years but it received the attention of researchers in early 90s and since then continuous research is being carried out in this field [3]. Depending on the type of strain induced, the mobility increase factor varies. In uniaxial strained silicon MOSFET only hole mobility increase is more prominent while in biaxial strained MOSFET both hole and electron mobility increases [4]. Improvement in mobility leads to improvement in carrier velocity and drive current of the device. In this

paper circuits designed with single and dual channel biaxial strained silicon MOSFETs is analysed. Single channel strained MOSFET has a tensile strained silicon channel [5] while a dual channel strained MOSFET has both a tensile strained silicon channel and a compressive strained silicon germanium channel and thus it shows even better performance than single channel strained MOSFET [6]. Due to the presence of compressively strained silicon germanium channel, dual channel strained MOSFET shows greater improvement in hole mobility than single channel strained MOSFET. Therefore, dual channel strained MOSFET shows superior performance than single channel strained MOSFET. Due to the improved performance circuits designed with these strained silicon MOSFETs also shows great improvement in performance. The inverter designed using biaxial strained silicon MOSFETs incurs low power, high noise margin and performs faster when compared to circuits designed with bulk MOSFETs.

In this paper among all VLSI circuits inverter is taken to analyse the performance of circuits designed with strained silicon MOSFETs since it is the most basic component to be used in designing of almost all analog and digital circuits in its original form or as a buffer. The analysis is done by simulation in sentaurus TCAD tool [7]. The structure of the MOSFETs taken in the circuits is also designed in TCAD tool.

MOSFETs are taken of 40 nm channel length and the germanium mole-fraction taken to introduce strain in the channel is 0.3. The rest of the paper is organized as follows. Section 2 of the paper gives an overview of the device design and the structure of the MOSFETs using 2-D device Sentaurus simulator. Section 2 also provides the simulation setup taken to simulate the MOSFETs structure and inverter circuit. Section 3 deals with results and discussion. Finally Section 4 provides the conclusion.

DEVICE DESIGN AND SIMULATION SETUP

The device dimensions and physical parameters of n-MOSFET and p-MOSFET in inverter are taken to be same. Figure 1 and Figure 2 shows the schematic cross-section of biaxial strained single channel and dual channel MOSFET respectively.

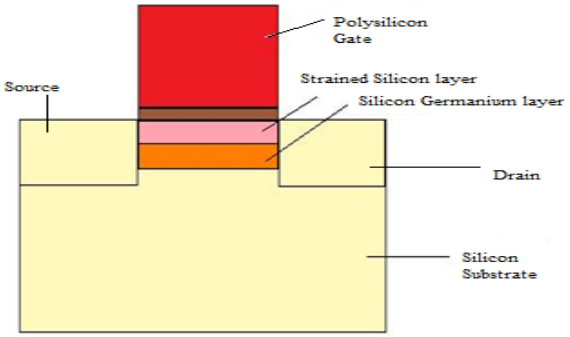

Fig. 1 Schematic Cross-Section of Biaxial Strained Single Channel MOSFET

The MOSFET structures are made in structure editor of Sentaurus TCAD tool. In biaxial strained single channel MOSFET a silicon

substrate is taken and in the channel region this silicon is replaced with a relaxed silicon germanium layer of thickness 10 nm
on which a strained silicon layer of thickness 10 nm is grown.

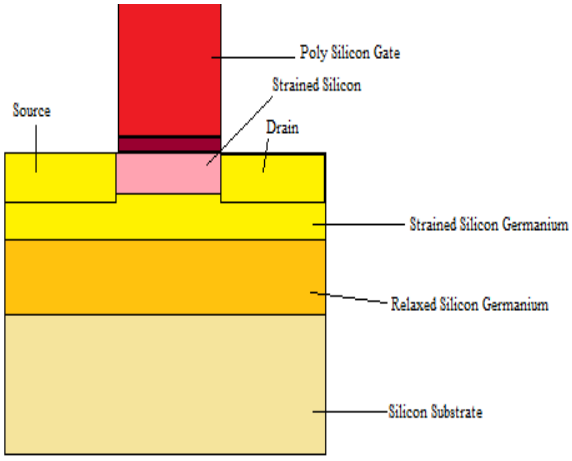

Fig. 2 Schematic Cross-Section of Biaxial Strained Dual Channel MOSFET

The strain induced depends on the mole-fraction of germanium in silicon germanium layer. The mole-fraction of germanium in the device is taken as 0.3. In dual channel strained MOSFET firstly a silicon substrate is taken over which a relaxed silicon germanium layer of thickness 70nm followed by a strained silicon germanium layer of thickness 10 nm and then a strained silicon layer of 10nm thickness is placed. The germanium mole-fraction to realise a relaxed silicon germanium layer is taken as 0.3 and for strained silicon germanium layer is taken as 0.8. The strained silicon germanium layer results in a compressively strained channel and strained silicon layer results in a tensile strained channel therefore, overall resulting in dual channel strained MOSFET.

The oxide thickness in these structures is taken as 2 nm on which poly gate of 40 nm thickness is placed. The source and drain region is implanted to a junction depth of 25 nm. The doping concentration in the substrate and channel region is taken as 5e+17cm^{-3}. The source and drain region are highly doped to the order of 1e+19 cm^{-3} for negligible parasitic resistances in this region. Figure 3 depicts the I_d-V_g graph of the designed structural device. It is observed from the graph that dual channel MOSFET shows improvised performance to other two MOSFETs. The threshold voltage obtained for bulk MOSFET is 0.134 V, for single channel strained MOSFET is 0.103 V and for dual channel strained MOSFET it is 0.94V. The dual channel strained MOSFET has least threshold voltage due to the presence of compressive strained silicon-germanium layer underneath strained silicon layer.

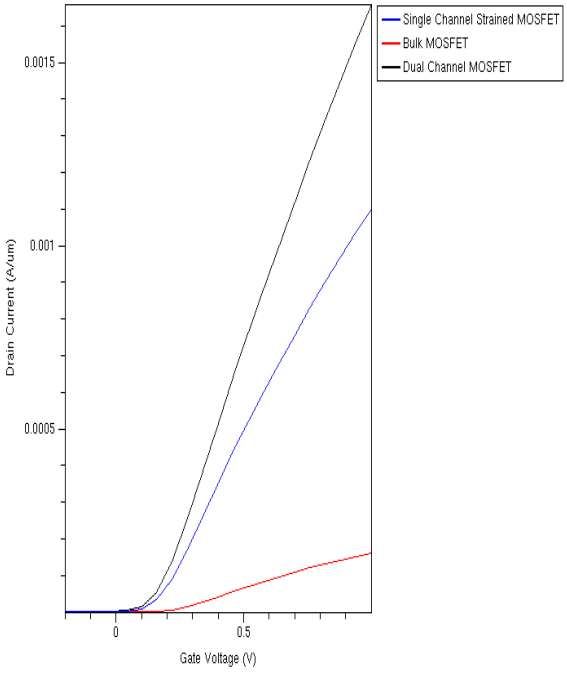

Fig. 3 Drain Current Plot with Gate Voltage

The extracted parameters of the above structures are taken in inverter circuit. The load capacitance in inverter is taken as 3e-14 F. Conventional bulk MOSFET of similar dimensions and parameters are also simulated for comparative study. The simulated strained silicon and conventional silicon n- and p-MOSFETs are connected for the design of CMOS inverters using the mixed mode simulator available in TCAD.

RESULTS AND DISCUSSION

Propagation Delay is one of the most important parameter which characterizes the operation of inverter. The propagation delay depicts the input-to-output signal delay during the high to low and low to high transitions of the output. The plot of the delay obtained for different V_{dd} is depicted in Figure 4.

It is observed from the plot that the propagation delay decreases with increase in V_{DD}. Single channel strained MOSFET has decreased threshold voltage as compared to bulk MOSFET. Therefore, the delay obtained for inverter designed with single channel strained MOSFET is lesser by a factor of 4% than bulk MOSFET since delay is inversely proportional to threshold voltage, V_{th}. The delay in inverter designed with dual channel strained MOSFET is more than single channel strained MOSFET and bulk MOSFET at low $V_{DD,}$ but with further increase in V_{DD} the delay decreases than both MOSFETs. This is because of the fact threshold voltage in dual channel strained MOSFET is higher than the other two MOSFET and as delay is inversely proportional to V_{DD}-V_{th}. Therefore, at low V_{DD} since the factor V_{DD}-V_{th} is low the propagation delays is more but with increase in V_{DD} the factor V_{DD}-V_{th} also increases and therefore the delay decreases even more than the other two MOSFET. Thus depending on the range of operation required for different applications, either of the strained silicon MOSFET can be selected. Overall, strained channel MOSFETs provide faster operation than bulk MOSFET.

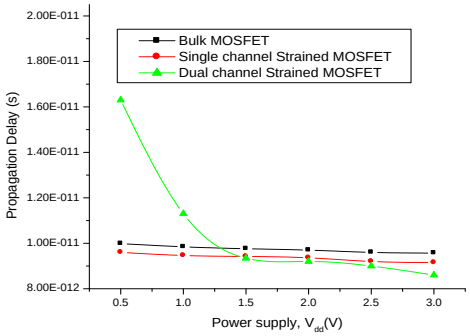

Fig. 4 Propagation Delay in Inverter

The Noise Margin for both the inverters is also calculated. The equation for low and High Noise Margin is:

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

Where,

$$V_{IL} = (2V_{OUT} + V_{T,P} - V_{DD} + K_R V_{T,N}) / 1 + K_R$$

$$V_{IL} = (V_{T,P} + V_{DD} + K_R (2V_{OUT} + V_{T,N}) / 1 + K_R$$

$$K_R = K_n / K_p.$$

$$V_{OL} = 0$$

$$V_{OH} = V_{DD}$$

As we know the higher the noise margin the better the circuit is and therefore, the results obtained depicts that the noise margin of strained channel MOSFET inverter is better than bulk MOSFET. Noise Margin is a kind of immunity of the circuit to noise and therefore, since strained channel MOSFET Inverter has high noise margin, it is more tolerant to noise and can be used in many VLSI applications where noise-free operations are required. Both NM_L and NM_H is calculated and plotted in Figure 5 and Figure 6 respectively.

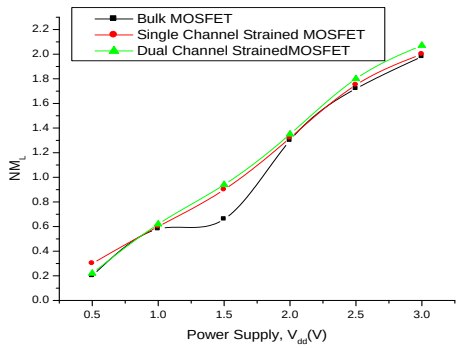

Fig. 5 NM_L with V_{DD}

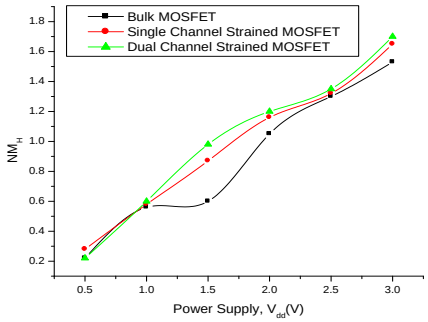

Fig. 6 NM_H with V_{DD}

It is observed from the plot that Noise Margin increases with increase in supply voltage and dual channel strained MOSFET has the highest noise margin. Therefore, strained channel MOSFET has better noise immunity than bulk MOSFET.

We have observed that strained channel MOSFET inverter shows improvement in performance with respect to delay and noise margin. Even when power dissipation is taken into account it is observed that strained channel MOSFETs inverter consumes less power as compared to bulk MOSFET inverter. This is because of the fact that in strained channel MOSFET less barrier lowering is observed and therefore due to more conduction band energy level very less conduction current is observed in static state resulting in less power consumption. Bulk MOSFET inverter conducts current even when no input is applied. This results in more static power dissipation in bulk MOSFET inverter. Figure 7 depicts the plot of static power dissipation. It is observed from the plot that bulk MOSFET inverter has more static power dissipation than strained channel MOSFET. Dual channel strained MOSFET inverter shows even less power consumption than single channel strained MOSFET inverter.

Therefore, strained channel MOSFET inverter shows much better performance in all aspects when compared to bulk MOSFET. Also dual channel MOSFET is superior to single channel MOSFET in terms of performance but in terms of fabrication cost it incurs more cost. Therefore, depending on the requirements we can use either single channel

strained MOSFET or dual channel strained MOSFET.

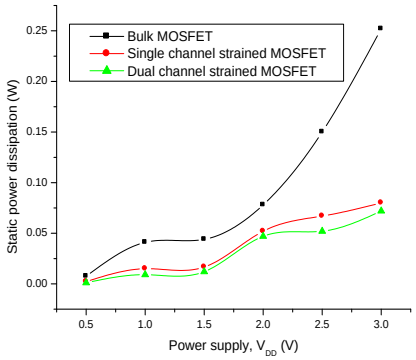

Fig. 7 Static Power Consumption of the Inverter

CONCLUSION

Strained channel MOSFET inverter shows less delay, high noise margin (noise immunity) and low static power dissipation. At low V_{DD} single channel strained MOSFET shows least delay but with increase in V_{DD} dual channel strained MOSFET shows least delay. Dual channel strained MOSFET has the highest noise margin and therefore, highest noise immunity. Strained channel MOSFET even consumes less static power. Therefore, it can be concluded from above results that strained channel MOSFET is superior to bulk MOSFET in all performance aspects and therefore, should be incorporated in the designing of modern digital VLSI circuits.

ACKNOWLEDGEMENTS

I express my deep sense of gratitude to E&CE Department of NIT, Hamirpur for extending their kind help and co-operation throughout and for providing me TCAD Sentaurus tool and other simulation facilities in the VLSI laboratory of the department.

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