

Automatic Switch cum Fuse IC for Low Voltage, Low Power, High Performance Current Conveyors

Ashutosh Tripathi

Amity School of Engineering & Technology, Amity University Jaipur, Rajasthan
India

ABSTRACT

The paper focuses on the analysis of switch cum fuse IC in signal processing. In signal processing it is proposed to prevent the damage of main IC from the external electrical fluctuations which are common in -these days. The proposed FUSE IC is also able to act as fuse for many times for main IC so that it can prevent the damage. It's like the work of MCB but a step ahead that we don't need to set back the switch in ON position again as like the MCB. It work as a array of multiple fuse which are so arranged that as one fuse goes off automatically another comes in the action and hence the power supply to main IC remains uninterrupted and the main IC remain after all the electrical fluctuations. In current conveyors are capable of operating at supply of & 1.0 V with rail-to-rail input and output voltage swings. Structure operates as linear circuit element and has a bandwidth of 60 MHz for 1.2 μ m CMOS technology.

Keywords: Signal Processing, MAIN IC, control signal, FUSE IC, Fuse Gate

Author for Correspondence E-mail: ashu20034@gmail.com; Tel: + 91-9694403636

INTRODUCTION

The FUSE IC consists of circuit which acts as a fuse for the main IC. In the condition of electrical fluctuation, these fluctuations can damage [2] [6] main IC and that damage is basically the burning of some gate in main IC. To prevent such type of hazard the IC circuit should have some sort of fuse, but fuses [1] [3] (common used wire fuse) are not as viable for electronic circuits and also MCB's are also not a good alternative for such circuit. Although, it makes the operation quite good but it is a bulky device. So the solution that comes out is, to fabricate a device which can work as a fuse. The FUSE IC provides a secure environment [4] for standby mode system IC's and makes the main circuit more reliable and increase the life span of main circuit. In the proposed IC the fuses are physically the AND gate [5] which behaves like a mediator

between power supply of main IC and the main IC itself. In the situation of electrical fluctuation AND gate burned out and behave like a fuse.

CIRCUIT DESCRIPTION

The whole circuit is consisting of FUSE part:-

In FUSE IC the following part, (shown in figure (1)) is responsible for protecting the main IC from electrical fluctuations. This part can also be stated as FUSE PART of this IC .When the fluctuations comes, internally a fuse (Gate) gets burned and makes the next levels of fuse circuit switch on, so that MAIN IC can work without any problem for many times.

The number of fuse circuit is decided by need of application that is, according to the need

number of fuses can be increased to any number

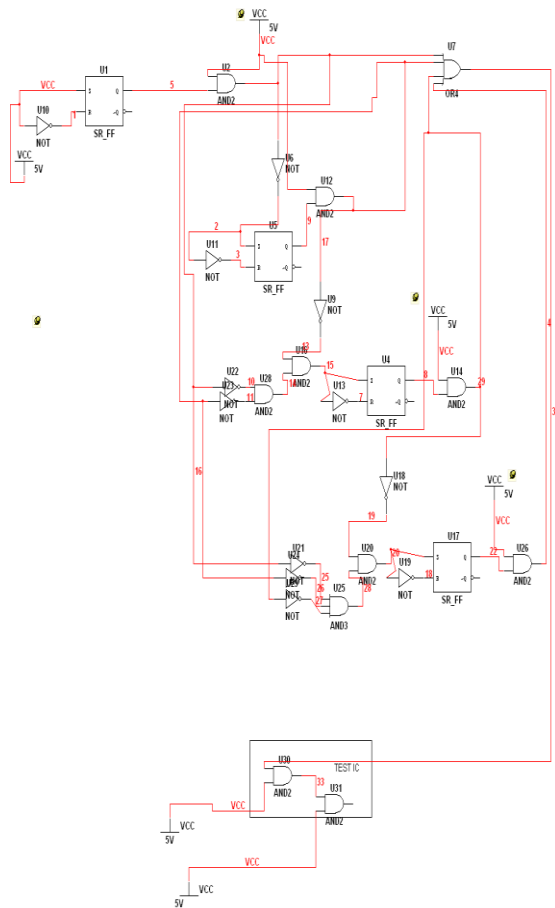


Fig. 1 Fuse Section of Fuse IC

After the not gate (U18) the level can be increased more by adding just the identical circuit as the level-3 of FUSE IC circuit's Fuse section posses.

In the circuit the operation starts when first of all switching on the MAIN IC so that it can start its normal operation. An external +Vcc supply is connected to the SR flip flop at level-1 for starting the fuse section operation. The circuit is so designed that only one level will be in operation at a time and rest will be at standby mode. When the gate (which is working as fuse here) of LEVEL-1 burned

out (the gate which is interfacing with MAIN ICs +Vcc e.g.:- for level 1 its U2),the level 1 comes out of the operation and automatically level 2 gets activated and the process is continued until all gates are not burned out in the fuse section.

RESULTS

Using MULTISIM 10, the simulated outputs and the following results are obtained:-

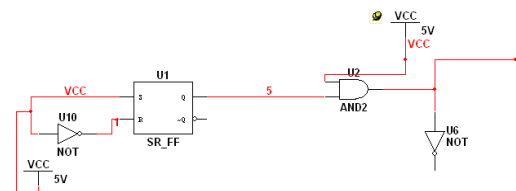


Fig. 2 Gate Diagram of Level-1 in Fuse IC

The starting level of the circuit is shown in Figure (2). A SR flip flop is governed by the control signal which is given by external +Vcc (i.e. 5V) supply. The supply will make S=1 and R=0 which make this flip-flop operational. As this flip-flop comes into operation it makes Q=1 and the AND gate (U2) starts working as the following truth table:-

A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1

The AND gate (here U2), behave like a fuse. Gate's one port is assigned to the output of the SR flip-flop and second port is assigned to +Vcc of the MAIN IC. If some fluctuations comes in the supply of MAIN IC then the AND gate (U2) fuse goes off. Now fuse level 2 of the IC comes to action.

The following is the level-2 of the fuse section:

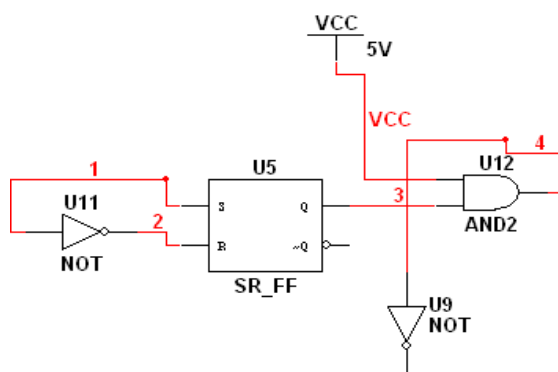


Fig. 3 Gate Diagram of Level-2 in Fuse IC

Now when the previous fuse level goes off and supply to the MAIN IC cutoff, level 2 comes into action so that the power supply to MAIN IC remains uninterrupted. As the level-1 fuses off the signal to output of SR flip-flop at this level becomes zero. A NOT gate is used to make this signal inverted so that next stage of SR flip flop comes in action(i.e. the next level of fuse). When the output from NOT was zero (i.e. previous circuit was in operating mode) the FF is set so that the output of it become $Q=0$. Now considering that the level -1 is burned out and level 2 is in operating mode, then $S=1$ and $R=0$ which makes $Q = 1$ and the output from FF goes to the AND gate(U12). One port of AND gate (U12) assigned to the output of SR

Flip-Flop and second port is assigned to +Vcc of the main IC. U12 works as fuse on this level and Output of this U12 goes to the MAIN IC as +VCC.

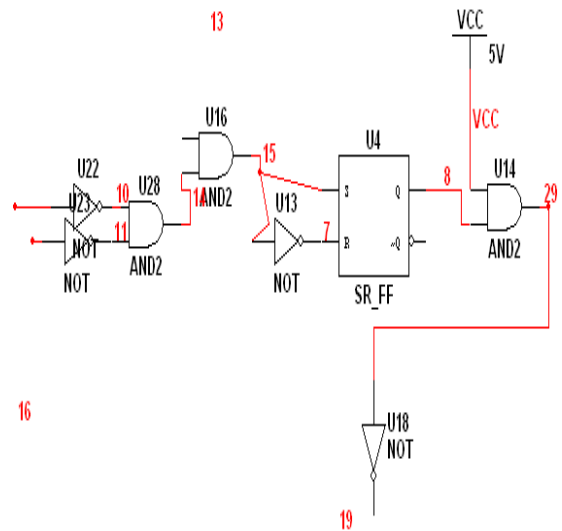


Fig. 4 Gate Diagram of Level-3 in Fuse IC

Figure (4) shows the level 3 of the fuse section. After failure of level-2, level-3 comes in action. As the previous level fuse burned out next level comes into action with the help of an inverter gate. Here the task of inversion is fulfilled by inverter U9. It makes the signal high to make possible the operation on the next level. Here we use a typical combination of NOT gate (U22, U23) and AND gate (U28) for checking the previous circuits (i.e. level-1 and level-2) weather they are fused or not. This circuit's importance becomes more because it prevents the start of level-3 until the previous two are not burned out properly. When it is ensured that previous levels are fused off then it produces high output and support the output of NOT (U9) so

that both can make HIGH output through AND (U16). The output of this AND (U16) is given to FF such that S=1 and R=0 so that Q=1 and makes the MAIN IC again operational. Output from the FF (U4) is applied to AND gate (U14) and another port of this gate is assigned to +Vcc supply of main supply. Output of this is applied to MAIN IC as its +VCC.

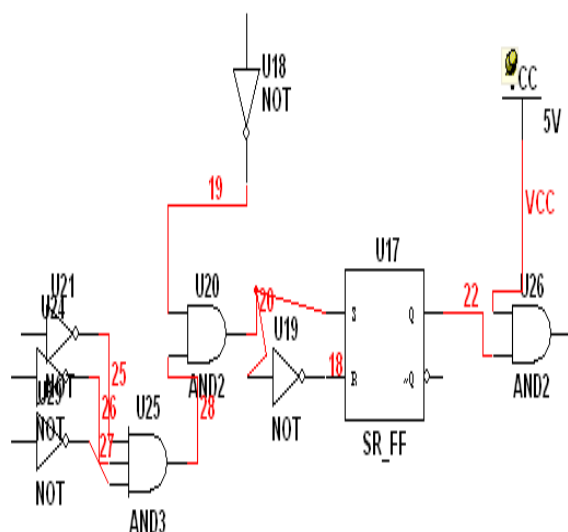


Fig. 5 Gate Diagram of Level-4in Fuse IC

Figure (5) Shows next level of circuit which is come to operation when level-3 is got fused. Here the difference between level-3 and level-2 is in the typical combination of NOT gates and AND gate, that is here the number of NOT gates are same as the number of previous levels and according to this rule the next level (i.e. level-5) is comprise of 4 NOT gate combination and combination is followed by next levels also.

So the general rule can be stated as the number of NOT gate in this typical combination is equal to the number of level

on which the circuit is operating (i.e. the present level of operation):- $(N-1)$

CIRCUIT DIAGRAM

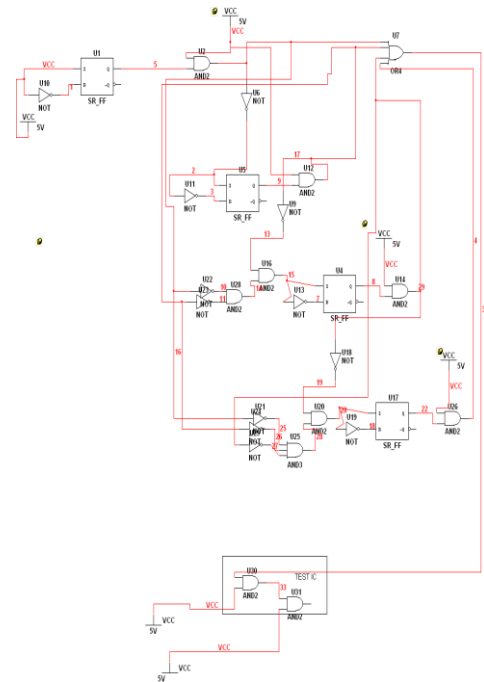


Fig. 6 Gate Diagram of fuse IC

CONCLUSION

The FUSE IC is capable of preventing damage from the external electrical fluctuation. The FUSE IC is perfectly analyzed for standalone system. FUSE IC is fully functional as a fuse for MAIN IC. The IC is thus, very useful for increasing the life span of the main IC. The IC can be implemented for the processors protection environment.

REFERENCES

1. Berberich S. E., Marz M., Bauer A. J. et al. Fraunhofer Inst. of Integrated Syst. & Device Technol., Erlangen. *Active Fuse, Power Semiconductor Devices and IC's* ISPSD 2006. IEEE International Symposium.
2. *Single Event Latchup Protection Of integrated Circuits* By P. Layton, D. Czajkowski, J. Marshall, H. Anthony, R. Boss Maxwell Technologies Microelectronics.
3. *Zener Zap Anti-Fuse Trim in VLSI Circuits* by Donald T. Comer*, Brigham Young University, Provo. UT 84602. (Received 23 October 1994; In final form 10 April 1995)
4. Galloway & Johnson. *Catastrophic Single-Event Effects in the Natural Space Environment* IEEE Nuclear and Space Radiation Effects Conference Short Course. 1996.
5. ADS7805 Data Sheet, Linear Products Burr-Brown IC Data Book. 1996.
6. Cliffe R. J., Brown J. & Smith I. R. *Journal of Physics D: Applied Physics* January 17th, 2001. 34. 1740–1742p.