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Design of a 10-bit Segmented Current-Steering CMOS D/A Converter for High Speed Communication System

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ABSTRACT

In the present work, design of a 10-bit digital-to-analog (D/A) converter using current segmentation architecture in 0.35 µm double-poly, four-metal, CMOS process has been attempted. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are 0.8 and 2.5 least significant bits (LSBs) respectively. For sampling frequency of 12-MSample/s, the spurious free dynamic range (SFDR) is better than 56 dB for signal up to Nyquist rate. The worst case power consumption is 58 mW and it operates with a single supply voltage of 3.3.

Keywords: *Digital-to-analog converters, binary weighted, matching, current-steering, CMOS*

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1. INTRODUCTION

The fast growing area of telecommunication has been forcing electronic industries to integrate both digital and analog circuits on a single chip. Mostly, current-steering digital-to-analog converters are used for many communication systems such as cellular base stations, cable modems, video signal processing, computer graphics and Bluetooth [1, 3, 5]. Current-steering D/A, in which output of an array of current sources is steered to the output resistive load directly depending on the digital input code, is commonly used for these high speed applications.

For above applications, D/A must fulfill specifications of bandwidth, resolution, spurious-free dynamic range (SFDR), signal-to-noise ratio (SNR) and DNL and INL. Also, low power consumption and reduced area are preferred for portable systems.

Thermometer architectures of current-steering D/A converter have guaranteed monotonicity. The matching requirement is significantly less, 50% matching of the unit current source results in a DNL < 0.5 LSB [1]. The drawback of thermometer architecture is that as the number of bits increases, the area increases significantly. On the other hand, the binary architectures consume N-binary-weighted current-source area for realization. In binary architecture, the output can change by more than 1 LSB, causing potentially substantial glitch, because at the midcode transitions, the current from the current sources corresponding to MSBs and LSBs flow in opposite direction. So, there are many trade-offs between thermometer and binary architectures. Section II discusses optimum D/A converter segmentation for given static parameters. Section III describes D/A converter building blocks. Section IV presents results from measurement, and Sec. V summarizes the conclusions.

2. ARCHITECTURE OF A 10-BIT CURRENT-STEERING D/A CONVERTER

A current-steering D/A converter can be designed either using binary-weighted current source or unary current source. Advantages and disadvantages of each architecture are available in literature [1, 2] and are summarized in Table I. To get the best of topologies, segmented current-steering D/A converter is the most preferred architecture.

Table I: *Comparison between Unary and Binary-Weighted D/A Converters.*

High Resolution CMOS Current-Steering D/A Converter		
	Binary Weighted Current Source	**Unary Weighted Current Source**
INL	=	=
DNL	–	+
Glitch	–	+
Monotonicity	–	+
Power	+	–
Area	+	–
Complexity	+	–

The DNL and INL will vary from the specified values because of any variation in the drain current of current sources and due to finite output resistance of sources particularly the one involved with LSB. Hence, it is required to select optimum segmentation. Lin and Bult [1] have done the area analysis for 10-bit resolution for different values of INL (0.5, 1.0, 2.0 LSB) and for DNL = 0.5 LSB.

From the plot for INL = 2.0 LSB and DNL = 0.5 LSB as given in [1], the optimal value of segmentation is found to be 60%, i.e., 6 bits of thermometer and 4 bits of binary type for the implemented current-steering D/A converter. The block diagram for 10-bit segmented current-steering D/A converter is given in Figure 1.

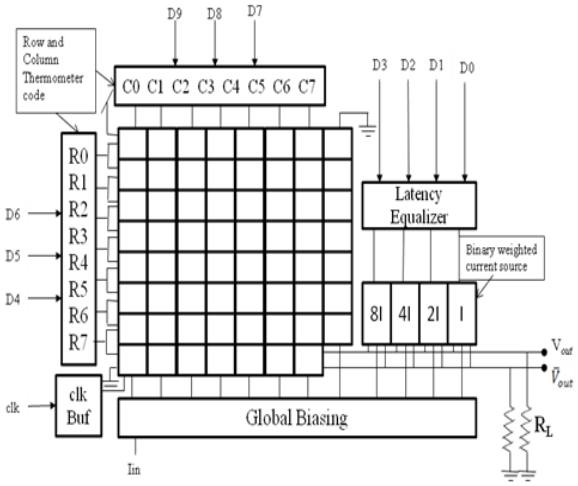

Fig. 1: *Block Diagram of 10-Bit Segmented Current-Steering D/A Converter.*

3. D/A CONVERTER BUILDING BLOCK

The circuit consists of a 4-bit binary and a 6-bit unary sub-D/A converter. There are three main functional sub-circuit entities in the architecture.

First, the decoder processes the applied bits in the appropriate way. For the 6-bit MSBs (D4-D9), the input bit streams are converted to a 63-bit thermometer codes. Converted thermometer codes switch $(8 \times 8-1)$ unary current sources, which produce appropriate current corresponding to the input binary pattern. In binary LSB, a dummy decoder has been added

to minimize latency problems between the signals generated by the MSB decoder.

The second part of the data converter is the current cell. This is the analog part of the chip. The mismatch error among these current cells is responsible for static errors and nonlinearity, if any, behavior of the D/A converter.

The third part is the latch sub-circuit, which interfaces the digital circuit to the analog circuit. It provides a synchronizing driver circuit for the switch. The design of the driver latch for high speed is a critical issue to achieve a good dynamic specification in the D/A converter.In the next sections, current cell and latch will be discussed in further detail.

3.1. The Current-Source Cell

The circuit of one unit current-source cell is shown in Figure 2. The analog part in current cell consists of cascoded current source (CS) with differential switch. All the cells are connected at node V and VB. Appropriate switching will guide the resulting current from array of current sources to nodes V and VB generating a linearly variant voltage across the resistors.

Cascode current structure provides large output resistance to serve as a better constant current source. The n-well, which houses the PMOS current sources, provides the isolation of substrate noise due to ground bounce. Also, dummy switch removes charge feed during switching.

Current-source design in a CMOS current-steering segmented D/A converter determines the static and dynamic behavior. For a current-steering D/A converter, the INL is mainly determined by the current matching of the current sources. A parameter INL yield is defined as the ratio of the number of D/A converters with an INL smaller than ½ LSB to the total number of tested D/A converters [2]. Based on the statistical mismatch model of [4], a relation exits between the CS transistor area, its overdrive, and its relative accuracy.

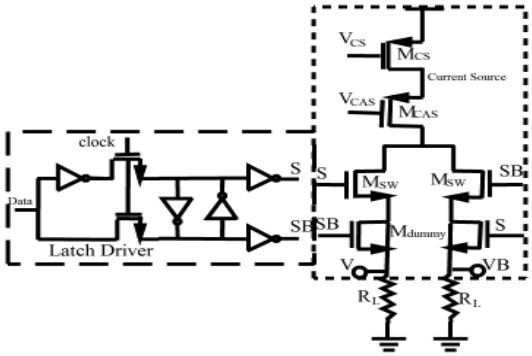

Fig. 2: *Unit Current-Source Cell.*

$$\left(\frac{\sigma(I)}{I}\right)^2 = \frac{1}{2(W_{cs}L_{cs})}\left(A_\beta^2 + \frac{4A_{VT}^2}{V_{OD}^{CS^2}}\right) \quad (1)$$

A_β and A_{VT} are the mismatch constants for large signal gain and threshold voltage respectively, $\sigma(I)/I$ is the standard deviation of a unit current source and depends upon resolution and yield [6]. The dimension of the current-source transistor is given by:

$$W^2 = \frac{I}{2K_P\left(\frac{\sigma(I)}{I}\right)^2}\left[\frac{A_\beta^2}{(V_{gs}-V_T)_{cs}^2} + \frac{4A_{VT}^2}{(V_{gs}-V_T)_{cs}^4}\right] \quad (2)$$

$$L^2 = \frac{K_P}{2I\left(\frac{\sigma(I)}{I}\right)^2}\left[A_\beta^2(V_{gs}-V_T)_{cs}^2 + 4A_{VT}^2\right]$$

Providing large gate overdrive voltage to the current source results in less area consumed by the current-source array. However, the value of $(V_{gs}-V_T)_{cs}$ is limited by the fact that both cascode transistor M_{CAS} and switch transistor M_{SW} have to operate in saturation [6]. The condition for the sum of the overdrive voltages is given by [6]:

$$V_{od}^{CS}+V_{od}^{CAS}+V_{od}^{SW}>V_{dd}-V_{O}^{\max} \quad (3)$$

Using Eqs. (2) and (3), the dimensions of the current-source transistor and gate voltage of all transistors can be found for given overdrive voltages. Rest of the parameters are the dimensions of switch and cascode transistors. These dimensions should be chosen to satisfy the impedance required for proper dynamic performance.

3.2. Latch (Driver) Selection

There are three basic causes for the dynamic performance degradation of a current-steering D/A converter associated with latch circuit in current cell [2].

1. Imperfect synchronization of the control signals at the switches.
2. Drain-voltage variation of the current-source transistors.
3. Coupling of the control signals through C_{GD} of the switches to the output.

Various latch (driver) circuits to minimize these effects are proposed in the literature [2, 3, 7, 8]. Major improvement in latch is increasing output crossing point to ensure that the two switching transistors are never simultaneously switched off. Giga latch [2] gives higher crossing point as well as highest speed. Latch in [7] reduces glitch energy for large-value current sources. But finger approach used in [7] uses number of delay buffer to switch current source, which consume large silicon area. The latch given in Figure 3 can be designed to achieve a high crossing point for several hundred mega hertz. Selection of $W_P < W_N$ for latch transistor and $W_P \approx (K_p/K_n)W_N$ for latch output inverter gives a high crossing point.

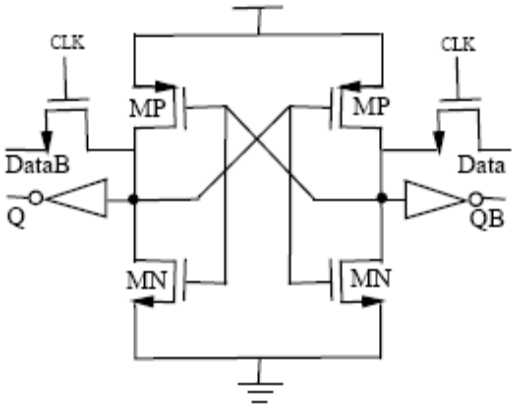

Fig. 3: *Latch Driver Circuit.*

Figure 4 shows a chip microphotograph of the realized design. It shows different parts of the design. In A, the 4-bit binary current-source array is shown. Area B shows unary current-source current cell for the 6-bit thermometer code; column thermometer decoder is in C. Area D and E, respectively, show clock driver and latency equalizer.

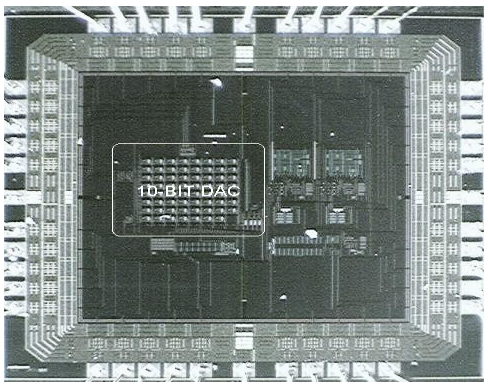

Fig. 4: *Microphotograph of the Realized Chip.*

4. MEASUREMENT RESULTS

All measurements have been performed for 1.5 V output swing. The analog voltage supply is 3.3 V, while the full-scale output current is 750 µA in all measurements.

Figure 5 shows the measured complementary output ramp for 1024 digital code with 1.5 V output swing. Measured differential nonlinearity (DNL) profile versus input code and integral nonlinearity (INL) profile of the 10-bit CMOS D/A converter are shown in Figure 6 and Figure 7 respectively. The DNL error lies between + 0.8 and − 0.65 LSB. The INL is smaller than ± 2.5 LSB.

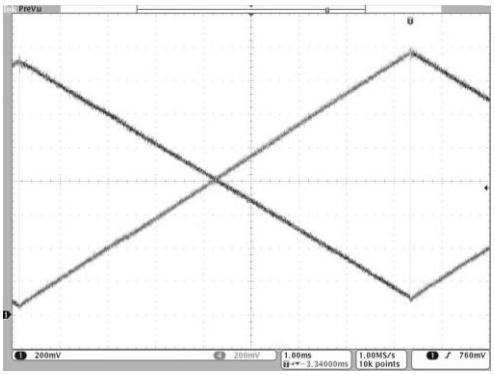

Fig. 5: *Measured Complementary Output Voltages.*

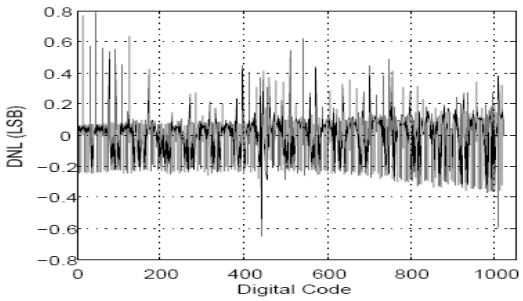

Fig. 6: *Measured DNL Profile versus Input Code.*

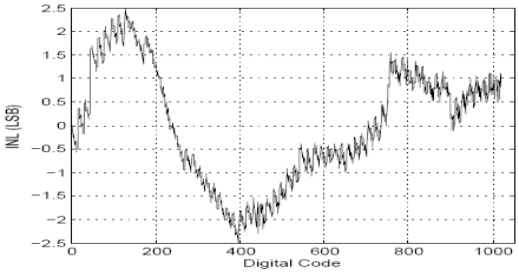

Fig. 7: *Measured INL Profile Versus Input Code.*

The D/A converter output spectrum has been measured for 500 KHz and 6 MHz signal frequency with 12-MSample/s update rate. For all the measurements, an SFDR better than 56 dB has been measured up to the Nyquist frequency. Figures 8 and 9 show some typical measured output spectra for the chip operating at a 12-Msample/s clock rate and, respectively, for a 500-KHz and for 6-MHz output signal frequency.

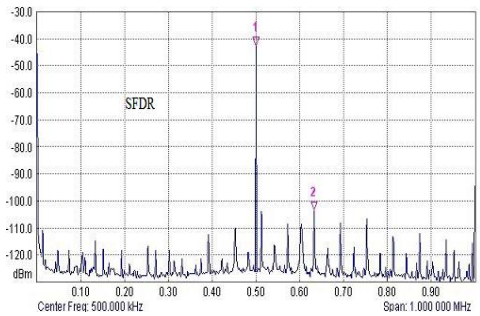

Fig. 8: *Output Spectrum for a 500-KHz Signal at 12-Msample/s Clock.*

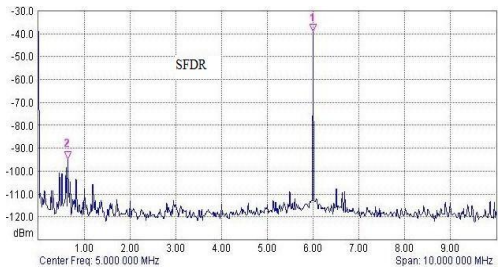

Fig. 9: *Output Spectrum for a 6-MHz Signal at 12-Msample/s Clock.*

Table II: *Performance Summary.*

Resolution	10-bit
Clock rate	Up to 12 S/s
DNL	< 0.8 LSB
INL	< 2.5 LSB
Offset voltage (μV)	63
SFDR (6 MHz@12 MS/s)	55.6 dB
Analog/digital supply	3.3 V
Power consumption (worst case)	58 mW
Silicon area	0.45 mm^2
Technology	0.35 μm CMOS

Table II summarizes the measured parameters of the 10-bit segmented current-steering CMOS D/A converter for 12-MSample/s clock.

5. CONCLUSIONS

In this paper, a 10-bit segmented digital-to-analog converter is designed and tested at 12-MSample/s. The optimum segmentation found in this design is six thermometer-coded bits in the MSB section and 4 bits in the LSB section. The D/A converter was implemented in a 0.35 μm, double-poly, four-metal, 3.3 V, standard CMOS process, occupying 0.45 mm^2 area. For clock rate up to 12-MSample/s, this design shows an SFDR better than 55.6-dB, even for signals close to Nyquist rate.

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