Journal of VLSI Design Tools and Technology
Volume 2, Issue (1-3), Compilation 2012

STM JOURNALS

An Innovative Approach of the Analysis of the Low Noise of a CMOS-Based Amplifier for Analog Signal-based Applications

Rajinder Tiwari*, R. K. Singh
Department of Electronics & Comm. Engineering, Kumaon Engineering College (KEC), Dawarahat (Almora), Uttarakhand, India

ABSTRACT

A low-noise amplifier (LNA), which is based on the cascode feedback methodology, has been commonly used for various wireless protocol-based network applications nowadays. It is so because this topology ensures that the low-noise amplifier (LNA) can achieve quite a high performance and thus, provides a high qualitative output. This amplifier is operated with a low voltage supply in the range of few volts that requires that the impedances of the input and the output to be rather of matched value so as to provide the output with minimum possible noise distortion. Thus, based on this concept/approach, an innovative approach of the design methodology for the design of a CMOS-based low-noise amplifier (CLNA) has been put forward for discussing the performance of the system. Now, in this efficient procedure of the design of CLNA, one has to consider the effective behavior of certain dominant parameters of the circuit such as noise figure, gain, linearity, channel length, etc. The simulation work of the proposed LNA has been carried out with pSpice software using the level 3 parameters based on 0.13 µm CMOS technology that provides the desired outputs. From these experimental results, it has been observed that with the input referred noise of the proposed amplifier 2.5 nV/Hz, the bandwidth of the circuit is in the range of 1 GHz, the power dissipation due to various devices is about 160 µW, with 0.5 dB of low-noise figure and the power consumption in the circuit is as low as 7.0 mW.

Keywords: *Low-noise amplifier (LNA), CLNA, CMOS devices, noise figure, pSpice, induced gate noise, CMOS-based amplifier, passive network*

****Author for Correspondence*** E-mail: trajan@rediffmail.com, rksinghkec12@rediffmail.com

1. INTRODUCTION

Recently, the wireless communication domain has made a tremendous progress with a rather rapid speed. It is highly desirable that a communication system should be highly integrated and it should provide more functions with optimized power consumptions that provide highly efficient output. The CMOS-based technologies are widely exploited and are commonly deployed in the area of the LNA within the acceptable range of RF signals, i.e., few Hz–GHz range. The CMOS-based low-noise amplifier (CLNA) is getting its popularity among the different wireless protocols for the transformation of the data applications such as GSM, PCS, IMT-2000, and Wireless LAN. The most dominant parameter that affects the overall performance of the LNA is the noise figure (NF).

This means that it is highly desirable by the amplifier that the noise figure should be minimized so as to obtain the desired performance level for a system, i.e., the NF value of the amplifier should be of low value such that the possibility of the distortion of the output signal of an amplifier should be nullified. However, this methodology of obtaining high performance of the amplifier requires that the size of the components should be of more consideration which in turn

enhances the systems overall cost in terms of much more power dissipation as compared to others [1–3]. One of the alternate solutions to this problem of analyzing the noise parameter of the amplifier is based on the use of the commonly used architecture, i.e., common source configuration-based amplifier. This designing approach has got an inbuilt advantage that it can be easily implemented for any specific applications, so as to realize the input matching and the best possible revised isolation. However, it has been observed that the noise figure of an amplifier has got a dominant impact on the performance of the amplifier with an extent of a bit large magnitude in case of practical applications. Another designing approach of an LNA, i.e., a low-noise amplifier can be implemented by adopting an architecture known as a cascode technique with a feedback topology.

This technique of LNA design is very common in use because of higher forward gain and revises isolation. It has got an inbuilt drawback that the substrate parasitic capacitance of common source topology will degrade the gain and noise figure of the amplifier [4–6]. This problem can be minimized with the use of an inter-stage matching circuit and a feed-back network so as to enhance the performance of the LNA circuit. The upcoming advent in the CMOS technology offers a highly favorable platform for the high-volume production of a broad range of consumer applications that requires the wireless communication. Hence with this introductory discussion, we can put forward that the designing process of the LNA involves trade-offs among gain, bandwidth, noise, power consumption, and linearity. It means that we have to optimize the designing approach with caution since these tradeoffs are quite complex in nature, and thus, adequate techniques have to be used that lead towards the acceptable level of performance of the amplifier [7–10].

2. BASIC AND CONVENTIONAL LOW-NOISE AMPLIFIERS

The advancement in the communication trends has put forward an extreme requirement of the CMOS solutions that can be very well associated with the transmitting and receiving of the data at quite high speeds with low error rates, low cost and low power consumption and dissipation. The basic sources of the presence of the noise in case of an amplifier may be because of the induced gate noise that primarily occurs at high frequencies. This sort of source of the noise distortion generally occurs in the amplifier when the channel thermal noise is capacitively coupled to the gate of the CMOS transistors of the circuit [11–13]. The effect of induced gate noise on the performance of the LNAs was so far usually, considered theoretically, i.e., mathematical calculations were done so as to find the overall impact of this on the performance of the LNA. This concept of the discussion is totally, based on the transistor sizing over all levels of inversion and channel lengths that form the important foundation base or the advanced CMOS design [14–16].

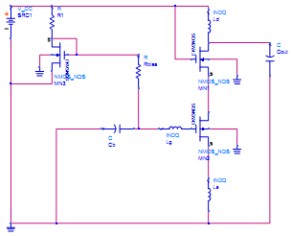

Fig. 1: *Basic Schematic of Low-Noise Amplifier* [10].

Figure 1 shows the schematic arrangement of a low-noise amplifier using MOS transistors. The design of this circuit is based on the concept of the cascode topology with source degeneration. The mathematical relation of the values of the inductors used in the circuit can be expressed as follows [17–20]:

$$L_s = \frac{R_s}{\omega_T} \cdot \frac{C_{GG}}{C_{GS} + C_{OV}} \text{ and } L_G = \frac{1}{\omega_\partial . C_{GG}} \quad (1)$$

where the value of the resistance connected with source is in the range of 50 Ω and the slew rate of the amplifier is efficiently high as required by the application [21].

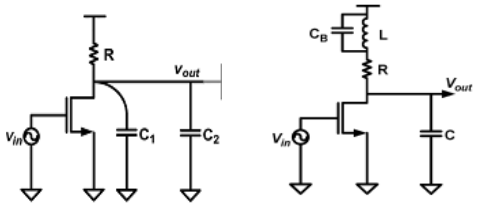

Fig. 2: *Basic Configurations of Amplifiers* [15].

Thus, based on this discussion one can easily deduce that this domain of analysis of the noise in case of amplifiers has got the maximum use in the domain of data transmission, i.e., the communication field. Transmission of data can be done with the help of any protocol that could be wireline-based or it could be wireless. It means that the wireline devices that operate at 10–40 Gb/s such as MUX and DEMUX circuitry arrangement for Ethernet applications demand the efficient and optimized design of broadband amplifiers [22–25].

The CMOS technology proves to be a better aspect in this problem since it has the capability of minimizing the parasitic limitations that enhances the performance of amplifiers and hence motivates to the use of bandwidth extension techniques such as distributed amplification for specific issues. However, on the contrary, these distributed amplifiers consume large area and high power and thus prove to be difficult and tedious to design owing to delay line losses. Figure 2 shows the schematic concept of the circuit arrangement of the configuration which is commonly used in the design of an amplifier for communication-based applications. This circuit consists of basic MOS transistor having the load resistance and other passive components that represent the drain parasitic and load capacitance, respectively, which is quite extensively used in the design of certain amplifiers that are used in wireline applications. The mathematical behavior of the amplifier can be discussed with the help of following equations, i.e., the MOS drain current [26, 27]:

$$I_D = I_F - I_R = I_{SPEC}\left(i_f - i_r\right) \quad (2)$$

where the specific current is the normalization current and is given as

$$I_{SPEC} = 2.n.\beta U^2_T \quad (3)$$

where $\beta = \mu.C'ox.\frac{W}{L}$ is the gain factor, and W and L are the device width and length respectively, i_f and i_r are the symmetric forward and reverse normalized currents. And the terminal voltages are normalized to thermodynamic potential, i.e.:

$$U_T = \frac{K.T}{q}, \quad v_p = \frac{V_P}{U_T}, v_{s(D)} = \frac{V_{S(D)}}{U_T} \tag{3}$$

where the pinch-off voltage V_P and the slope factor n are the function of the gate voltage, i.e.:

$$V_P \cong \frac{V_G - V_{TO}}{n}, n \equiv \frac{dV_G}{dV_P} = 1 + \frac{\gamma}{2\sqrt{V_P + \phi}} \tag{4}$$

In Eq. (4), V_{TO} is the threshold voltage, γ is the substrate factor and ϕ amounts to twice the fermi- potential.

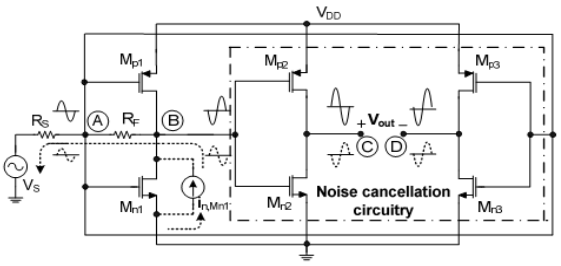

Fig. 3: *Schematics Arrangement of Basic* LNA [21].

It is a well known standard feature that CMOS inverter has no internal nodes, i.e., the performance of the circuits that are designed using CMOS transistors will not be degraded due to the presence of the extra parasitic poles and zeros, when operated at high frequency. Thus, this sort of designed circuits have good linearity relation existing in the voltage-to-current conversion and vice-versa.

Figure 3 shows another commonly used schematic arrangement of a low-noise amplifier with an inbuilt circuit arrangement of thermal noise canceling. It means that this circuit is highly capable of reducing the thermal noise at the output to an acceptable ratio. This means that this inbuilt circuitry arrangement of minimizing the thermal noise which is associated with the CMOS transistors in turn enhances the overall performance of the amplifier. It is also observed from Figure 3 that the circuit arrangement of this inbuilt circuitry of thermal noise canceling is quite easy since it consists of simple CMOS inverters [28, 29].

3. METHODOLOGY AND LOW NOISE ANALYSIS APPROACH

This has been in discussion since long that in order to achieve the high-performance of the device and the circuits which are used as VLSIs in logic and memory applications, the CMOS has become a quite popular and dominant technology due to its very low power capability and large noise margin [30–32]. This CMOS technology has also got an inbuilt feature of containing the analog and digital systems that is highly desirable in the designing and fabrication of the on-chip devices technology.

Since the signals of the circuits in VLSI systems are quite frequently used to drive the large parasitic capacitances, the minimizing signal swing of the noise or high sensing of the presence of the noise capability is highly required so as to improve the system

performance. The two most important features of the CMOS-based LNA circuit that are required in input matching circuit design are the passive component values and their quality factor. Thus, it has been observed that the high value of the passive components increases the chip size, while the low quality factor value increases the losses that in turn degrade the noise factor.

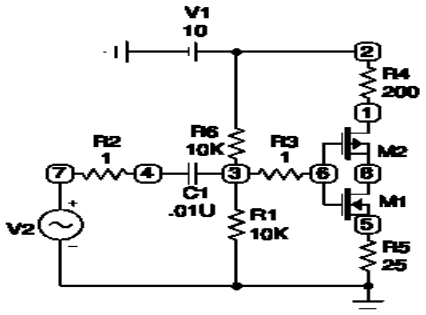

Fig. 4: *Proposed Schematic Arrangement of a Low-Noise Amplifier.*

Figure 4 shows the circuit arrangement of a novice CMOS-based low-noise amplifier which has got the inbuilt capability of analyzing the presence of the noise in the signal at the output. With this discussion, this work puts forward an innovative CMOS-based LNA with high performance that is very much capable of minimizing the noise at an acceptable level as per the need of the applications. The transistors M1 and M2 constitute the main module of the circuit which are used in the reduction of noise at the output.

For this purpose, there is no requirement of the matching between the common-source stage and the common-gate stage for the two transistors. In this circuit, the capacitor has been used as the blocking module that minimizes the unwanted signal from the output, i.e., a blocking capacitor [33]. Now in the analysis of the circuit of this proposed CMOS-based LNA, we have taken into account the most dominant parameters. Thus, the resultant impedance of the circuit can be discussed and the value of the impedance containing the L_f and the R_f can be expressed as:

$$L_f = (0.2 \square 5) R_f \tag{5}$$

$$Z_{in} = j\omega L_s + \frac{1}{j\omega(C_{gs1} + C_d)} + Z_{eff} + \frac{g_{m1} L_s}{C_{gs1}} \tag{6}$$

where C_{gs1} is the gate-to-source capacitance of M1, g_{m1} is the trans-conductance of M1, Z_{eff} represents the impedance of the matching network and $\dot{A}$ is the resonance frequency. With the available impedance of input source, the matching condition is [34–36]:

$$\frac{g_{m1} L_s}{C_{gs1}} = R_s \tag{7}$$

$$j\omega L_s + \frac{1}{j\omega(C_{gs1} + C_d)} + Z_{eff} = 0 \tag{8}$$

Now, it is a well-known and acceptable fact that the noise present in the signal of an amplifier is the prime source that limits the minimum signal level that a circuit of the amplifier can process with acceptable quality and performance. This whole philosophy of the amplifier is governed with the help of a predominant factor, i.e., known as noise figure of the amplifier.

The main role of the noise figure is to provide the optimized condition with which the amplifier can achieve the required performance,

STM JOURNALS

and this can be achieved with the proper selection of the appropriate device under the influence of power and gain of the amplifier. The simplified input-referred noise voltage power of each transistor of the circuit in Figure 4 can be given as [37]:

$$u_{nij}^{\ 2} = \frac{K_F}{C_{OX} W_{ij} L_{ij}} . \frac{1}{f} + \frac{4k_B T_\gamma}{gm_{ij}} \quad (9)$$

where K_F is the flicker noise coefficient, C_{OX} is the normalized oxide capacitance, W_{ij} and L_{ij} are the width and length of the transistor respectively, f is the frequency, k_B is the Boltzmann constant, T is the absolute temperature, γ is the coefficient equal to the 2/3 for long channel device and gm is the trans-conductance of the transistor.

The total input-referred noise spectral density is the sum of each input referred noise voltage (two times to account for the differential circuit) and is given by [38]:

$$u_{nie}^{\ 2} = 2.\left[\frac{R_{o1}^{\ 2}}{A_{o1}^{\ 2}} \left(u_{n12}^{\ 2} . g_{m12}^{\ 2} \right) + \frac{R_{o2}^{\ 2}}{A_{o1}^{\ 2} . A_{o2}^{\ 2}} \left(u_{n22}^{\ 2} . g_{m22}^{\ 2} \right) \right] \quad (10)$$

The total output noise power is proportional to $i_{sc}^{\ 2}$, i.e., the mean-square input port short circuit current [35, 36].

$$F = \frac{i_{sc}^{\ 2}}{i_s^{\ 2}} = \frac{\text{noise power due to source and amp}}{\text{noise power of source alone}} \quad (11)$$

where

$$i_{sc} = -i_s + i_n v_n Y_s$$

$$i_{sc}^{\ 2} = i_s^{\ 2} + \left(i_n + v_n Y_s \right)^2 - 2 i_s \left(\mathrm{i_{nt}}\, v_n Y_s \right) = 0 \quad (12)$$

Since i_s not correlated with i_n or v_n, thus, we have

$$F = 1 + \frac{\left(i_n + v_n Y_s \right)^2}{i_s^{\ 2}} \quad (13)$$

4. EXPERIMENTAL ANALYSIS AND SIMULATION RESULTS OF CMOS AMPLIFIER

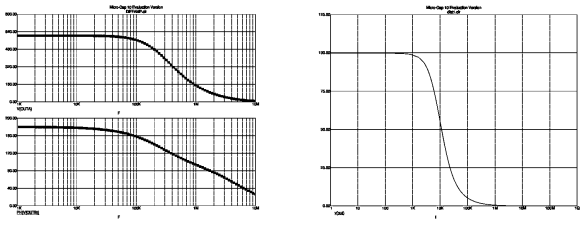

Fig. 5: *(a) AC Analysis (b) AC Analysis (Noise Distortion).*

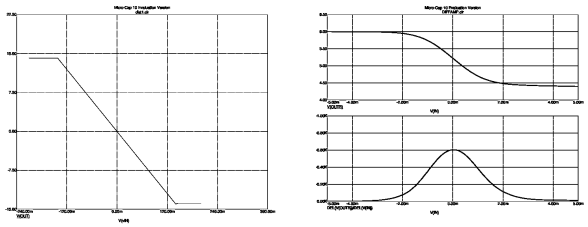

Fig. 6: *(a) DC Analysis (Noise Distortion) (b) DC Analysis.*

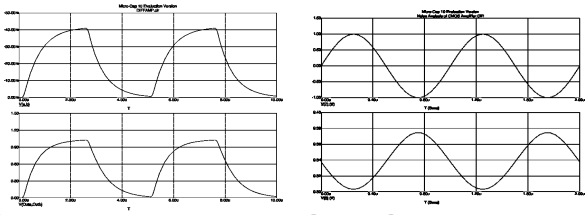

Fig. 7: *(a) Transient Analysis (b) Transient Analysis (Noise Distortion).*

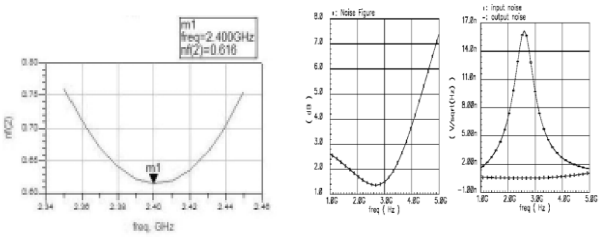

Fig. 8: *(a) Noise Figure of the Input and Output (b) Proposed LNA Noise Analysis.*

The above shown Figures (i.e., 5–8) give us a glimpse of the experimental results of the detailed analysis of the low-noise amplifier that are obtained with the simulation of the parameters using pSpice software based on 0.13 µm CMOS technology. Figures 5(a) and 5(b) present the experimental results of the AC analysis of the low-noise amplifier with and without the effect of the noise present in the signal.

Similarly, Figures 6 and 7 provide the analytic behavior of the proposed LNA circuit under the impact of the noise. Figures 8(a) and 8(b) show the behavior of the noise figure of the proposed LNA and the input-output behavior of the noise of the amplifier, respectively. The noise analysis summary shows the contributions of different noise sources in the total noise. This is a very powerful feature to focus the effort to improve the noise performance of the device which contributes the maximum noise. It has been observed that the maximum gain and minimum noise situation cannot be obtained at the same time.

5. CONCLUSIONS

In this work, an innovative concept of a low-noise amplifier (LNA) has been put forward that has been based on the cascode feedback topology. This LNA has got all the desired features and parameters which are required for any specific application with highest feasible performance. During the design process of this amplifier, several important factors have been keep in consideration, say the power consumption, gain, and noise figure of the amplifier so as to achieve the best results of the system with good performance.

In order to discuss the performance of the proposed low-noise amplifier circuit, the simulation work of the circuit has been carried out using pSpice software with a 0.13 µm CMOS technology. For this purpose, the circuit has been applied with a low supply voltage with the input and output impedances as 390 Ω and 45 kΩ, respectively. So, with these modeled parameters, the noise analysis of the low amplifier circuit has been performed that in turn provides the high performance at the output with large voltage gain, wide bandwidth, low input referred noise, and low power dissipation. In this circuit, the rise of the input referred noises at low frequency is attributed to the flicker noises of transistors. The noise floor, which extends over most of the amplifier bandwidth, comes from the channel thermal noises.

ACKNOWLEDGEMENTS

The authors are thankful to Prof. D. S. Chauhan (Vice Chancellor, UTU) for providing the environment for this work, Mr. Aseem Chauhan (Additional President, RBEF), Major General K. K. Ohri, AVSM, Retd. (Pro V. C., AUUP, Lucknow Campus), Prof. S. T. H. Abidi (Director, ASET) and Brig. Umesh K. Chopra, Retd. (Director, ASET) and Deputy Director

(ASET) for their kind cooperation, motivation, and kind and most valuable suggestions.

REFERENCES

1. B. Razavi. *IEEE Journal of Solid-State Circuits*. Sept 2002. 37(9). 1135–1145p.
2. K. H. Chen and C. K. Wang. *Proceedings of 2004 IEEE Asia-Pacific Conference on Advanced System Integrated Circuits*. Aug. 2004. 296–299.
3. A. Hee-Tae and D. J. Allstot. *IEEE Journal of Solid-State Circuits*. 37(8). August 2002. 985–993p.
4. B. M. Ballweber, R. Gupta and D. J. Allstot. *IEEE Journal of Solid-State Circuits*. Feb 2000. 35. 231–239p.
5. R. C. Liu, K. L. Deng and H. Wang. *IEEE Radio Frequency Integrated Circuits Symposium*. June 2003. 103–106p.
6. P. J. Sullivan, B. A. Xavier and W. H. Ku. *IEEE Transactions on Microwave Theory and Techniques.* October 1997. 45(10). 1969–1976p..
7. B. M. Frank, A. P. Freundorfer and Y. M. M. Antar, *IEEE Microwave and Wireless Components Letters*. 2002. 12. 327–329p.
8. K. K. Moez and M. I. Elmasry. *IEEE International Symposium on Circuits and Systems*. 2004. 1. 1048–1051p.
9. T. H. Lee. *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press. 1998.
10. A.-S. Porret. *Design of a Low-Power and Low- tage UHF Transceiver Integrated in a CMOS Process*. Ph.D. Thesis No. 2542. Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland. 2002.
11. A.-S. Porret and C. Enz. *SPIE International Symposium on Fluctuation and Noise*. Santa Fe. June 2, 2003.
12. [12] V. H. Varotto Baroncini and O. Da Costa Gouveia-Filho. *Proceedings of SBCCI*, Pernambuco, Brazil. September 7-11, 2004. 82–87p.
13. D. M. Binkley, C. E. Hopper, S. D. Tucker, et al. *IEEE Transactions on Computer-Aided Design of Integrated Circcuits & Systems.* February 2003. 22(2). 225–237p.
14. M. Bucher. *Analytical MOS Transistor Modelling for Analog Circuit Simulation*. Ph. D. Thesis. No. 2114. Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland. 2000.
15. A. J. Montalvo, R. S. Gyurcsik and J. J. Paulos. *IEEE Journal of Solid State Circuits*. Apr. 1997. 32. 535–543p.
16. [16] P. J. Hurst. *IEEE Transactions on Education*. Aug. 1992. 35. 253–261p.
17. P. R. Gray, P. J. Hurst, S. H. Lewis, et al. *Analysis and Design of Analog Integrated Circuits*. New York, NY. Wiley. 2000.
18. P. E. Allen and D. R. Holberg. *CMOS Analog Circuit Design*. Oxford University Press. 2002.
19. E. Sanchez-Sinencio, J. Ramirez-Angulo, B. Linares-Barranco, et al. *IEEE Journal of Solid State Circuits.* Dec. 1989. 24(6). 1576–1586.
20. H. J. Song and C. K. Kim. *IEEE Journal of Solid State Circuits*. 25(3). June 1990. 841–848p.

21. N. 1. Khachab and M. Isrnail. *IEEE Journal of Solid-state Circuits*. Nov. 1991. 26(11). 1689–1699.
22. S. 1. Liu and Y. S. Hwang. *IEEE Journal of Solid-state Circuits*.. June 1994. 29(6). 750–752p.
23. [23] S. 1. Liu and C. C. Chang, *IEEE Journal of Solid-state Circuits.* Sep. 1995. 30(9). 1025–1029.
24. G. Han and E. S. Sinencio. *IEEE Transactions on Circuits and Systems-II*. Dec. 1998. 45(12).
25. Z. Huang, Y. Inoue, H. Yu, et al. *IEEE Asia Pacific Conference on Circuits and Systems*. Dec. 2006. 708–711.
26. [*Star-Hspice Manual*. Avant Corp., Fremont, CA. July 1998.
27. B. Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill. 2000.
28. M. Egels, J. Gaubert, P. Pannier, et al. *Journal Of Electronics Letters*. 2004. 40(24). 1513–1514p.
29. H. S.Kim, et al. *Journal of Circuits and Systems*. 2000.˙42nd Midwest Symposium. 2. 1040–1043p.
30. Jie Long and Robert J. Weber. *Proceedings of the 17th International Conference on VLSI Design*. 2004. 393–397p.
31. F. Ali, C. Hutchinson and A. Podell. *Journal of IEEE Microwave and Guided Wave Letters*. Feb. 1992. 2. 70–72p.
32. Jihak Jung 1, Kyungho Chung1, Taeyeoul Yun1, et al. *Journal of. Microwave and Optical Technology Letters*. Jan. 2006. 203–205p.
33. Jiarui Lin. *Analogy High Frequency Electronics and Circuits.* Peking Publishing House of Science and Technology.˙1986. 151–153p. *International Journal of Electrical Engineering and Technology (IJEET)*. January–June 2012. 3(1). 165–172p. ISSN 0976- 6545 (Print) & ISSN 0976–6553 (Online). .
34. Rajinder Tiwari and R. K. Singh. *International Journal of Computer Engineering & Technology (IJCET)*. January–June 2012. 3(1).,147–153p. ISSN 0976–6367 (Print) & ISSN 0976–6375 (Online).
35. Rajinder Tiwari, R. K. Singh and Ganga Ram Mishra. *International Journal of Electronics & Communication Engineering & Technology (IJECET)*. May–July 2011. 2(2).,01–07p. ISSN 0976–6464 (Print) & ISSN 0976–6472 (Online).
36. Rajinder Tiwari and R. K. Singh. *International Journal of Microcircuits and Electronics (IJME)*. 2012. 3(1). 15–26p. ISSN 0974–2204.
37. Rajinder Tiwari, R. K. Singh and Ganga Ram Mishra. *Journal of Physical Sciences* (An International Research Journal of Physical Sciences). 2010. 2(1). 143–149p. ISSN: 0975–5519.