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Delay Minimization of 3 Cascaded Inverters with the Help of Logical Effort and Transistor Sizing

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ABSTRACT

With logical effort minimum delay of the path can be estimated by only knowing number of stages, path effort, and parasitic delay without the need to assign transistor sizes. This is superior to simulation where delay depends on sizes and you never achieve certainty that the size selected would offer minimum delay. In this work 3 cascaded inverters is being sized in the ratio 1:2:3 to achieve minimum propagation delay and comparison is made with the 3 cascaded inverter not sized in the ratio 1:2:3.

Keywords: *effort, 3 cascaded inverters, capacitance*

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1. INTRODUCTION

Logical effort is a method to make these decisions:

It uses a simple model of delay. Allows back-of-the-envelope calculations. Helps make rapid comparisons between alternatives. Emphasizes remarkable symmetries [1].

With logical effort minimum delay of the path can be estimated by only knowing number of stages, path effort, and parasitic delay without the need to assign transistor sizes. This is superior to simulation where delay depends on sizes and you never achieve certainty that the size selected would offer minimum delay [1].

This paper is summarized as follows: section A gives a brief introduction about how to compute path effort. Section B consist of proposed work and comparison of results.

SECTION A

Now computing the path effort:

F = GBH (stage effort)

Path effort $f = F^{1/N}$

Thus minimum delay of N stage path is

$$D = NF^{\frac{1}{N}} + P$$

This is a key result of logical effort.

$C_{in} = (g_i * C_{out})/f$

Starting with the load at the end of the path work backward applying the capacitance transformation to determine the size of each stage.

Check the arithmetic by verifying that size of initial stage matches the specifications. Once we get the input capacitance or gate capacitance we can determine the width of the transistor by applying:

$C_g = C_{ox*} W* L$= gate capacitance

Where, **$C_{ox}=(E_{ox}/t_{ox})$**

SECTION B

2. PROPAGATION DELAY OF 3 CASCADED INVERTERS

G=1 (logical effort [1])

H=20/1 (electrical effort)

B=1 (branching effort)

F=GBH=1*1*(20/1) = 20

$f=\sqrt[3]{F}=20^{1/3}=2.714$

Now tracing backward, input capacitance of the first inverter $\mathbf{z = (c_{out}*g_i)/f}$

20*1/2.714=**7.36**

This is the output capacitance for the second inverter so, the input capacitance of the second stage is:

X=7.36*1/2.714=2.714

Now verify the size of the third inverter:

X=2.714 would now act as output capacitance for third stage so we have assume the size of the third inverter to be 1unit putting the values in the above formula we get

(1*2.714) /2.714=1

Delay $D = N*F^{1/N}+\sum P = 3*2.714+3=$**11.114**

Where, N= Number of stages

P=parasitic delay of an inverter [1]

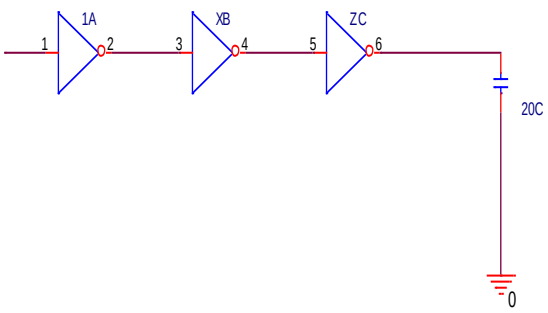

Fig1: *cascaded inverters*

Table I: *Parameter List and Values of 3 Cascaded Inverters not Sized in the Ratio 1:2:3.*

Parameters	Values
G	1
H	20
B	1
F	20
f	2.74
D	11.114

3. PROPOSED WORK

Delay depends on the number of input applied to the gate and the number of stages in the multistage network. As the number of input is reduced delay is reduced. In the proposed work the gate capacitances at each stage is very less when sized in 1:2:3 ratio and hence the delay is reduced [2].

What would be the effect on propagation delay if we size the inverters in the ratio of 1:2:3?answer to this question is if we increase the number of inputs ,gate capacitances C_g increases[1] , as a result delay increases.

Here we have assumed single input multistage n\w consisting of inverters only but this concept can be utilized in any multistage n\w so that rough estimate of the each component size can be made which would offer minimum

delay, prior to simulation. Assuming the size of first inverter to be X and Y=2X, Z=3X

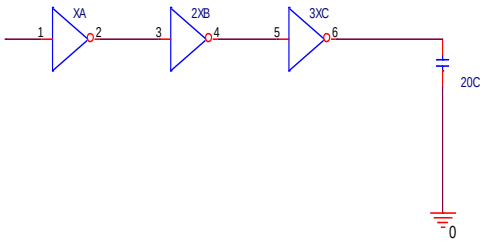

Fig2: *cascaded inverters sized in the ratio 1:2:3*

G=1 (logical effort [1])

H=20/X (electrical effort [1])

B=1 (branching effort [1])

F=GBH=20/X

$f=\sqrt[N]{F} = (20/X)^{1/3}$

Now tracing backward, input capacitance of the first inverter $\mathbf{z=(c_{out}*g_i)/f}$

$[20*1/(20/X)^{1/3}]=3X$, solving for X.

X=**3.85**

f=**1.75**

Since the path effort is reduced, delay is reduced.

D=3*1.75+3=**8.25**

Here X, Z, 2x, 3x are the gate capacitances C_g and

C_g is proportional to width of the transistor.

Also $C_g=C_{ox}$ W L Where, $C_{ox}=E_{ox}/t_{ox,}$

Table II: *Parameter List and Values of 3 Cascaded Inverters Sized in the Ratio 1:2:3.*

Parameters	Values
G	1
H	20/X where X=3.85
B	1
F	20/X
f	1.74
D	8.24

Thus the delay is reduced to **8.24** when the sizing is done in the 1:2:3 ratio.

4. CONCLUSION

From the study of logical effort we can conclude that this concept can be utilized in sizing the transistor in such a way that the delay achieved is minimum. This concept can be utilized in any multistage network consisting of NAND, NOR inverters etc. for delay minimization.

5. FUTURE WORK

Implementation of logical effort and transistor sizing in hierarchical designs and estimating the delay.

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