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High-speed CMOS ADCs Design

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ABSTRACT

This paper presents the design of high-speed subranging and flash analog to digital data converters (ADC) including the design of efficient operational amplifier to meet the performance requirements of these data converters for the specifications laid down targeted to the SCL 1.2 μm CMOS Foundry. The design starts from the specification of the circuit, its theoretical analysis for the parameter estimations of the transistors as well as the circuit's design. Its simulation studies with design iterations were carried out using EDA tools. Pre- and post-layout electrical behavior verification of the circuit was carried out for the circuits from its layout as well as netlist extracted circuit from its schematic. Best performance has been achieved by the design iterations as presented in the paper.

Keywords: *Flash and subranging ADC, operational amplifier, comparator and subtractor*

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1. INTRODUCTION

The paper discusses about the design of operational amplifier, comparator, voltage subtractor, high-speed flash and subranging data converters for the targeted technology. Since, the dramatic increase in complexity of integrated circuits poses an enormous design challenge, designing a multimillion-transistor circuit and ensuring that it operates correctly is a difficult task that is virtually impossible without the help of computer aids and well-established design methodologies. The level of circuit performance that can be reached within a certain design time strongly depends on the efficiency of the design methodology. Following are the major design styles generally used.

1.2. Full Custom Design

In this design style, the geometry and the placement of every transistor can be optimized individually. The designer designs all the circuitry and all interconnection paths. It requires a longer time until the design maturity can be reached, yet the inherent flexibility of adjusting almost every aspect of circuit design allows far more opportunity for circuit performance improvement, during the design cycle. The final product typically has a high level of performance and the silicon area is relatively small because of better area utilization. But this comes at a higher cost in terms of design time.

1.3. Semi Custom Design

The idea behind semi-custom design is to reduce the implementation effort by using a limited library of standard cells. The advantage of this approach is that the cells only need to be designed and verified once for a given technology and they can be reused many times, thus amortizing the design cost. In the early design phase, the circuit

performance can be even higher than that of a full custom design, since some of the components used in the semi-custom design are already optimized. But this offers less opportunity for performance improvement and the overall performance of the final product will inevitably be less than that of full custom design.

2. FULL CUSTOM DESIGN OF OPERATIONAL AMPLIFIER

Operational amplifiers are among today's most widely used circuit blocks in analog integrated circuit. It can be used as summers, integrators, differentiators, comparators, attenuators and much more. Defined generally, an operational amplifier is a high-gain differential input amplifier [1–4, 15–17]. Designers have been trying to integrate these versatile circuit blocks into rest of their circuitry since the mid-1960s. The μA709 was the first Op amp designed on an integrated circuit. The circuit of the operational amplifier, presented in Figure 1 is a two-stage operational amplifier consisting of a differential-stage gain and inverter-stage gain with negative feedback due to capacitor and it is a second order model for operational amplifier.

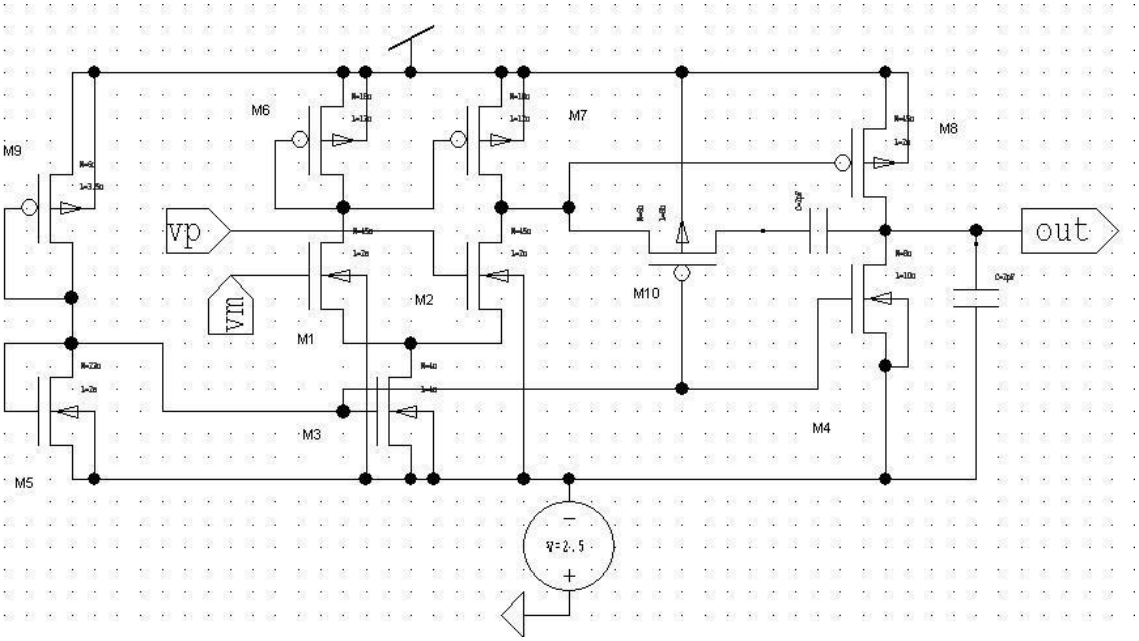

Fig. 1: *Schematic Architecture of an Operational Amplifier*

with an n-Channel Input Pair.

Theory: The transfer function model for the above circuit is,

$$A_{vCL} = A_{vo}(1 - s/z_1)/[(1 - s/p_1)(1 - s/p_2)] \quad (1)$$

$$PM = \tan^{-1}(\omega_{ugf}/z_1) - \tan^{-1}(\omega_{ugf}/p_1) - \tan^{-1}(\omega_{ugf}/p_2) - (-180) \quad (2)$$

$\forall\ z_1 = g_{ds10}/C_c$,

$p_1 = g_{ds2} * g_{ds3}/(g_{ds2} + g_{ds3})C_{gs4}$

$p_2 = (g_{ds8} + g_{ds4})/C_L$

$R_o = 1/gds_4 + gds_8$ (3)

$R_{oCL} = \beta * Ro/A_{vo}$ (4)

$SR = 2I_{ds1}/C_c$ (5)

$\omega_{ugb} = g_{m2}/Cc$ (6)

$A_{vCL} = Av(s)/[1 + \beta Av(s)]$ (7)

β: Closed loop feedback factor

$LG(s) = \beta\omega_{ugb} = \omega_{ugb} = A_{vo} * p_1 \quad \forall\ \beta = 1$ (8)

Settling time $(t_s) = 1/\omega_{ugb}$

$\ln(1/\varepsilon) = (1/A_{vo} * p_1)\ln(1/\varepsilon) = \tau\ln(1/\varepsilon)$,

$\forall\varepsilon < 1\%$ (9)

$CMRR = A_{vo}/A_{cm}$ (10)

$PSSR \pm = \pm \Delta Vref/\Delta Vout$ (11)

$ICMR(max) = Vref - Vtn_1 = Vdd - Vds6 - Vgd1$

$= Vdd - Vds6 + Vgs1 - Vtn1$ (12)

$ICMR(min) = Vtn_1 = Vds3 + Vgs1 = Vgs3 - Vtn3 + Vgs1$ (13)

$P_{dissipation} = Vsupp * Isupp (Vsupp)$ (14)

$Pout = \frac{1}{2} C_L V_o^2$ (15)

Specifications of operational amplifier are given in Table I.

Table I:

Parameters	**Values**
Open Loop Gain (A_v)	66.92 db
Phase Margin	87.49 °
F_{3db}	1.2 kHz
F_{GB}	6.54 MHz
ICMR	+ 2.49 V, − 1.17 V
Slew Rate	+ 5, − 2(V/μs)
$P_{Dissipated}$	0.9528 mW
V_{out} Range	+ 2.49 V, − 2.42 V
PSRR+	63.25 db
PSRR-	63.95 db
CMRR	147 db
Offset	− 6.64 mV
Output Resistance (R_o)	150 kΩ
Output Resistance in Closed Loop	6.82 kΩ

Sizes of Transistors based on calculations using above formulas are given in Table II.

Table II:

Transistor Name	L(µm)	W(µm)	V_{th} (V)	$g_m(\mu\Omega^{-1})$	$g_{ds}(\Omega^{-1})$	Ids(A)
M1	2	45	1	73	778 n	5 µ
M2	2	45	1	71	730 n	5 µ
M3	4	4	746 m	31	222 n	10 µ
M4	10	8	753 m	28	73 n	9 µ
M5	2	23	710 m	485	7 µ	171 µ
M6	12	18	− 732 m	19	199 n	− 5 µ
M7	12	18	− 735 m	19	205 n	− 5 µ
M8	2	45	− 650 m	116	4 µ	− 9 µ
M9	3.5	6	− 680 m	99	6 µ	− 171 µ
M10	8	6	− 958 m	302 f	36 µ	751 f

Following simulation results, presented in Figures 2 to 13 are used to determine the parameters of operational amplifier that is mentioned in Table I. Figure 2 is used to determine the phase margin and gain of the operational amplifier.

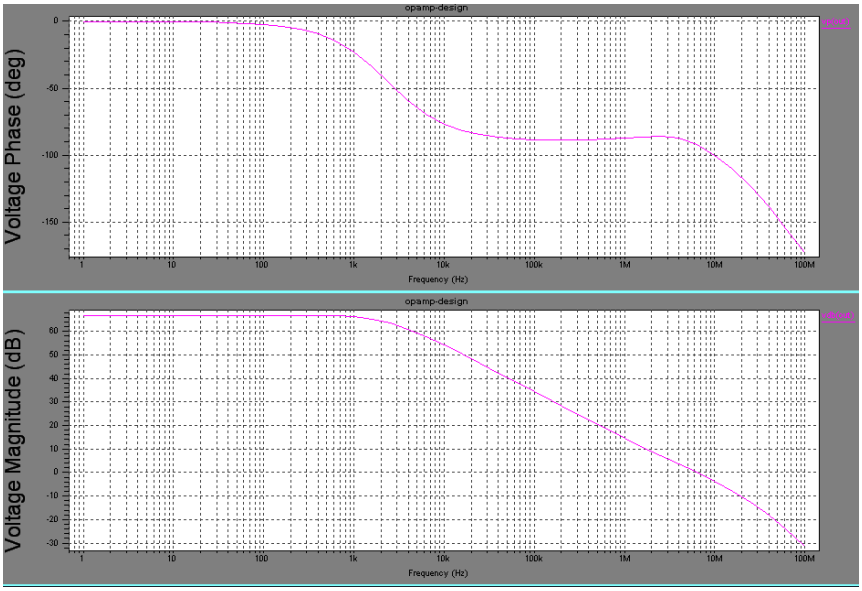

Fig. 2: *Frequency Response of Operational Amplifier.*

Probably, one of the biggest concerns with reduced power supplies is the ICMR. The ICMR is the input common-mode voltage over which the differential input works as desired. Even if the ICMR is sufficiently large, it is also necessary that it can be centered within the power-supply range. The ICMR is important because it determines if the output of a stage can interface with the input of another different or similar stage.

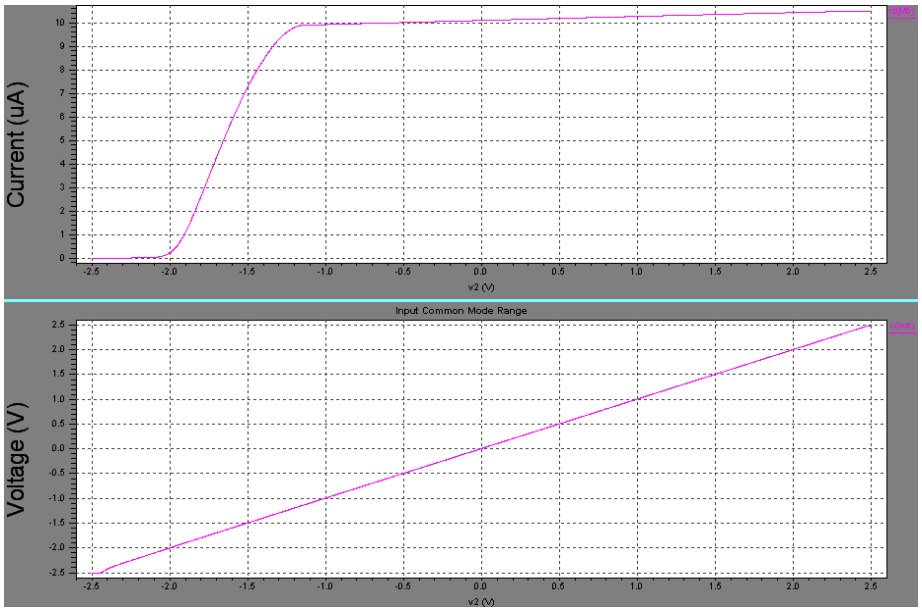

Fig. 3: *Input Common Mode Range of the Op Amp.*

The output of the op amp has several important limits, one of which is the maximum output current sourcing and sinking capability. There is a limited range over which the output voltage can swing while still maintaining high-gain characteristics. The output has also a voltage rate limit called slew rate. The slew rate is generally determined by the maximum current available to charge or discharge a capacitance. Normally, slew rate is not limited by the output but by the current sourcing/sinking capability of the first stage.

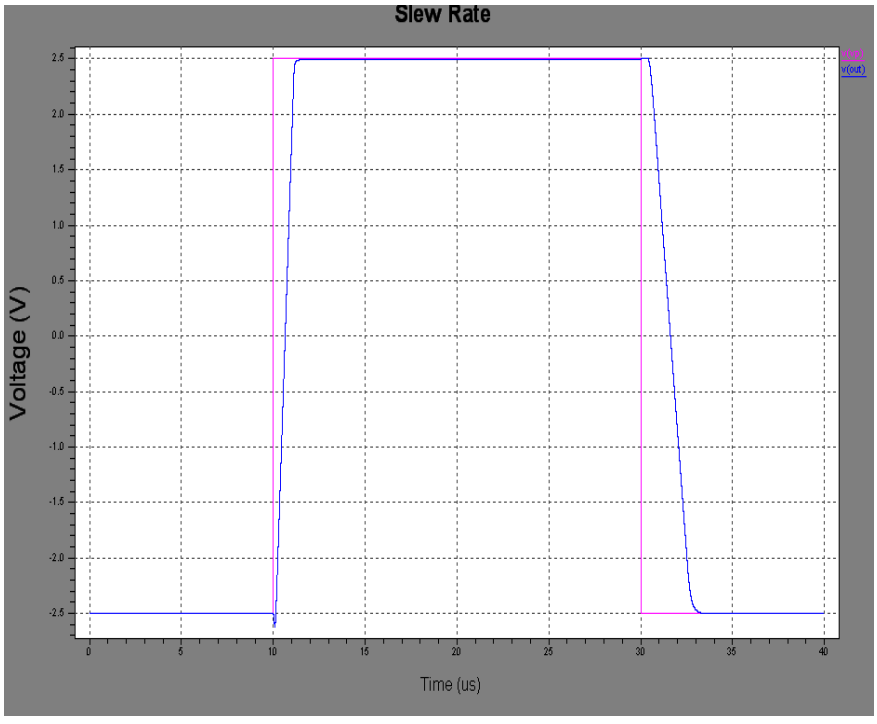

Fig. 4: *Slew Rate of the Op Amp.*

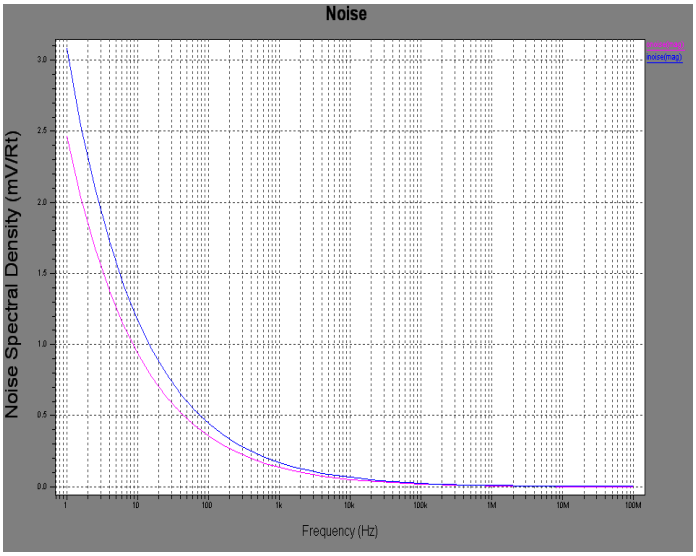

Fig. 5: *Noise Analysis for Input/Output Signals of Op Amp.*

$NF = (SNR)_{inp}/(SNR)_{op}$ (16)

$SNR = 20\log(S_{max}/N_{max}) = 20\log(2^N)$,

$N_{max} <= 1$ LSB (17)

$SNR = 20\ln(2^4) = 20 * 1.386 = 27.725$ dB (18)

Dynamic Range is the minimum to maximum output variation in the operational range.

DR = SNR

$= 6.012 * N + 1.76$ for N-bit ADC (19)

$DR = 6.012 * 4 + 1.76 = 25.80$ (20)

Other non-ideal characteristics of the op amp include the power supply rejection ratio, PSRR. The PSRR is defined as the product of the ratio of the change in supply voltage to the change in output voltage of the op amp caused by the change in the power supply and the open-loop gain of the op amp. Thus,

$PSRR = (\Delta V_{dd}/\Delta V_{out}) * A_v(s)$ (21)

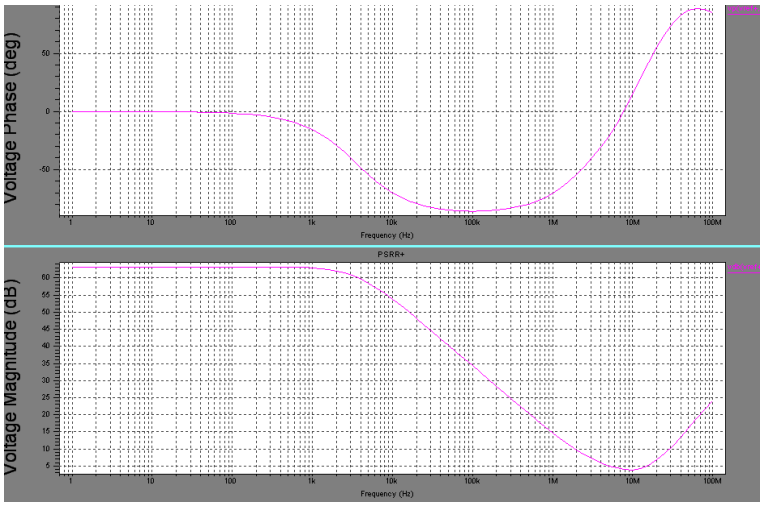

Fig. 6: *PSRR $^+$ of the Op Amp.*

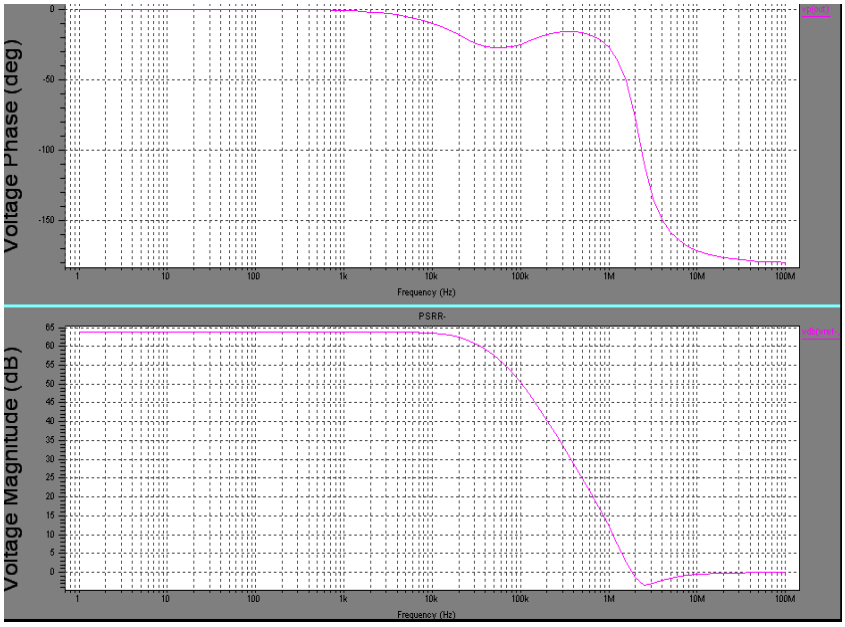

Fig. 7: *PSRR⁻ of the Op Amp.*

The output voltage swing of the op amp is range of the voltage over which the output swings from the negative saturation to positive saturation voltage value.

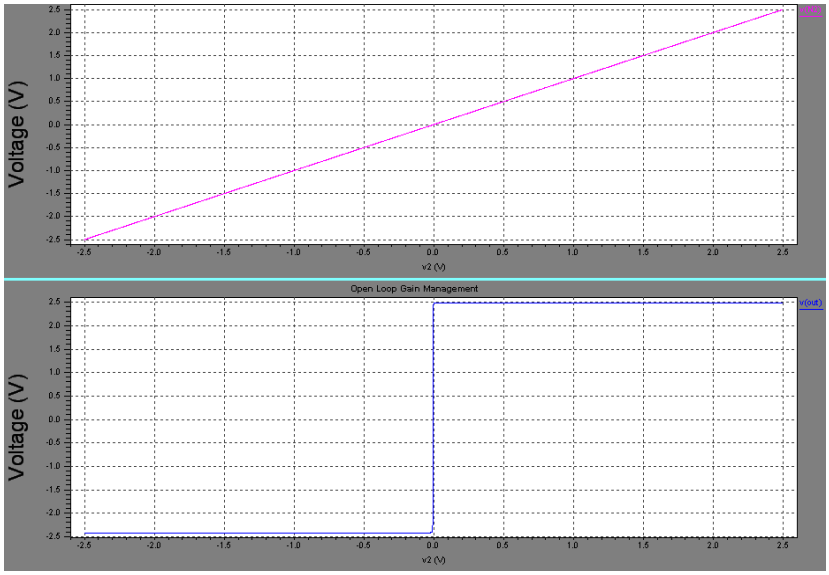

Fig. 8: *Output Voltage Range of the Op Amp.*

To check whether our op amp can function as a basic unity-gain buffer, connect the negative input to the output, and apply a sine wave (1 V amplitude, 1 kHz, centered at ground) to the positive input. Run a transient simulation that captures 2–3 complete cycles of the sine wave, and plot the input and output waveforms. The output should follow the input closely.

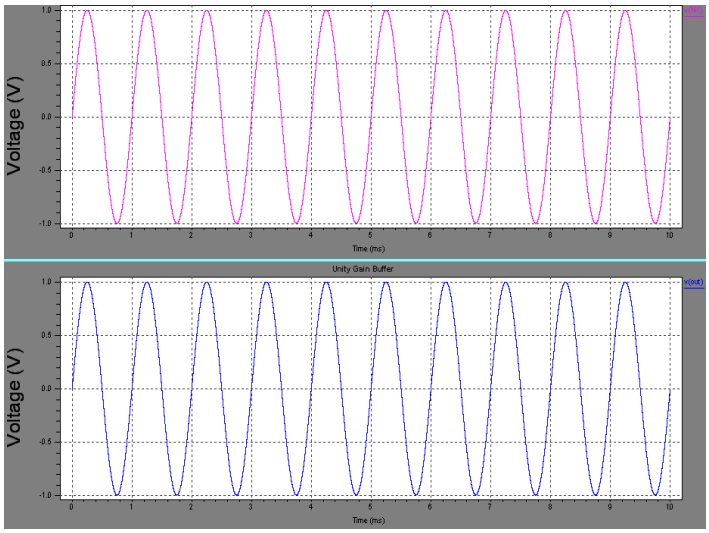

Fig. 9: *Op Amp as a Unity Gain Buffer.*

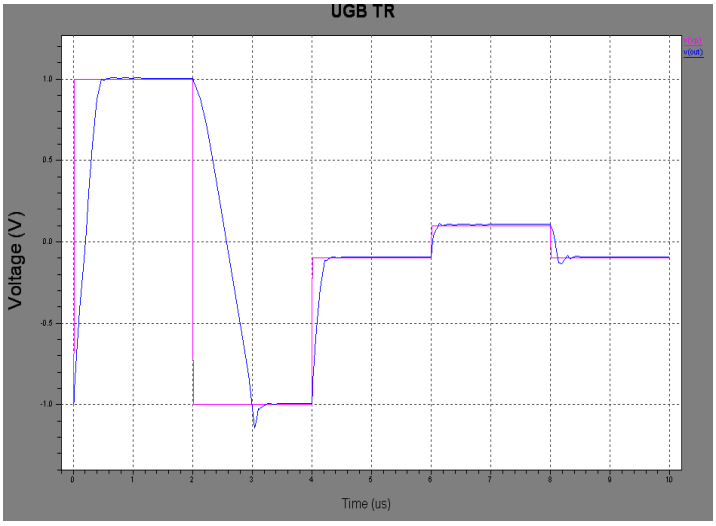

Fig. 10: *Unity-Gain Transient Response of the Op Amp.*

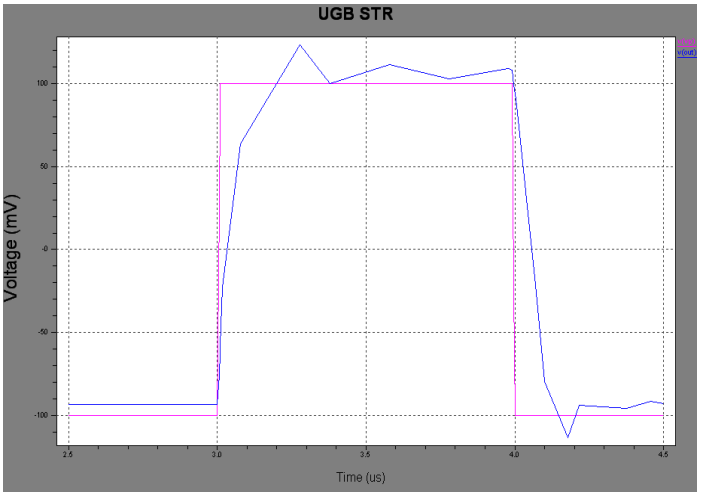

Fig. 11: *Unity-Gain, Small-Signal Transient Response.*

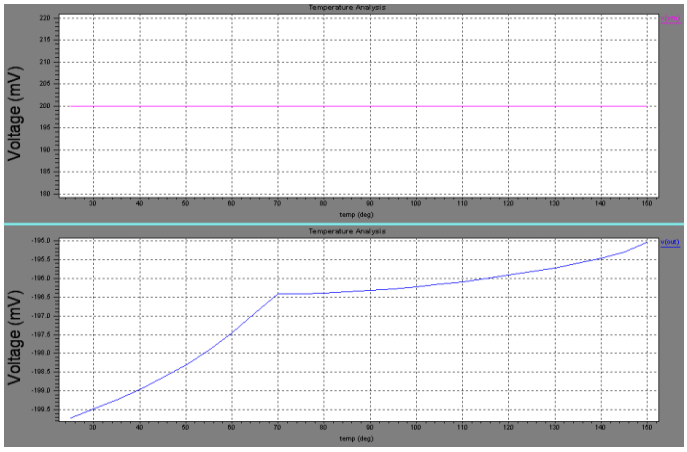

Fig. 12: *Thermal Response of the Op Amp with Changing Temperature.*

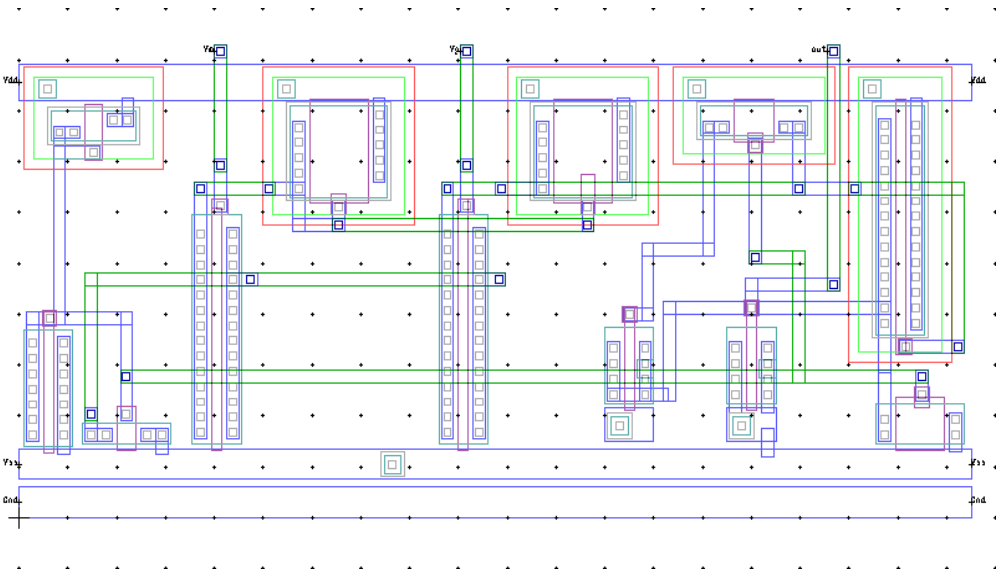

Fig. 13: *Operational Amplifier Layout in Outline Format.*

Core size = 195 * 89 μm, Core Area = 17355 μm^2

SCL 1.2 μm CMOS Technology Design Data:

C_{area_metal1} = 27 aF/Sq

C_{fringe_metal1} = 0.024 fF/Sq

R_{sh_metal1} = 0.05 Ω/Sq

C_{area_metal2} = 15.61 aF/Sq

C_{fringe_metal2} = 0.015 fF/μm

R_{sh_metal2} = 0.03 Ω/Sq

Abut Cell Height = 80 μm

R_{sh_Nwell} = 2130 Ω/Sq

$R = \rho L/A = \rho L/(W * t) = (\rho/t)(L/W) = R_{sh} * (L/W) = R_{sh} * ASR$ (22)

R_{sh} is the sheet resistance for the layer

ASR is the aspect ratio that is L/W of the layer

$Cox = \in_0 \in_{sio2}/t_{SiO2,}$ $C_T = C_{ox} * W * L$ = Total Gate Oxide Capacitance (23)

3. VOLTAGE SUBTRACTOR CIRCUIT DESIGN

Using a basic differential op-amp

configuration, a subtractor may be constructed as shown in Figure 14. The input signals can be scaled to the desired values by selecting appropriate values for the external resistors; when this is done, the circuit is referred to as scaling amplifier. However, in Figure 14, all external resistors are equal in value, so the gain of the amplifier is equal to 1.

The output voltage of the differential amplifier with a gain of 1 is

$$V_o = -(R/R) * (V_m - V_p) \quad (24)$$

i.e., $V_o = V_p - V_m$

Thus, the output voltage V_o is equal to the voltage V_p applied to the noninverting terminal minus the voltage V_m applied to the inverting terminal; hence the circuit is called a subtractor (Figure15).

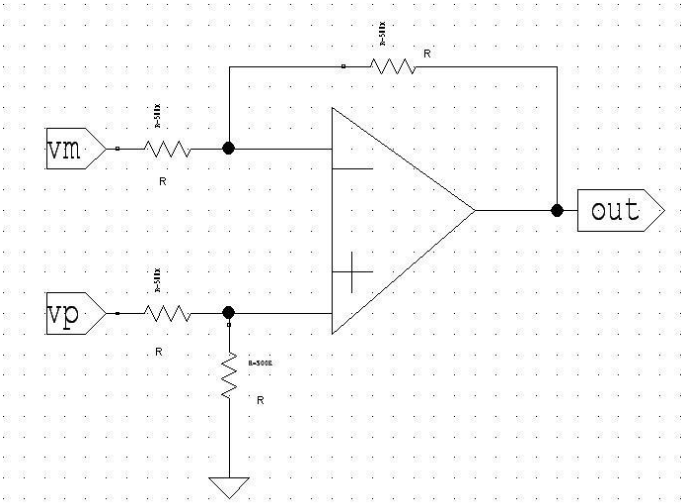

Fig. 14: *Voltage Subtractor Circuit.*

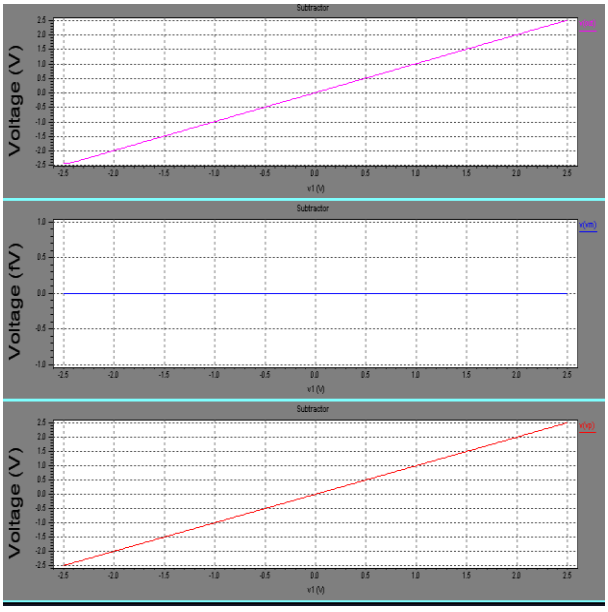

Fig. 15: *Subtractor Circuit Simulation Result.*

4. DESIGN OF ANALOG TO DIGITAL CONVERTER

Analog to Digital converters are the basic building blocks that provide an interface between an analog world and the digital domain. As it is the main block in mixed signal applications, it becomes a bottleneck in data processing applications and limits the performance of the overall system. Analog to digital converter (ADC) is a device that accepts an analog value (voltage/current) and converts it into digital form that can be processed by a microprocessor. The signal that we want to convert into digital form is applied to input while the reference voltage should be applied to V_{ref}. The output bits represent the input signal in digital form (Figures 16–21).

4.1. 4-Bit Flash ADC

Flash ADCs are also called parallel ADCs. Due to parallel architecture, it is the fastest ADC among all other types and is suitable for high bandwidth applications. It consumes a lot of power, has low resolution, and is expensive for high resolution. It is mainly used in high-frequency applications and in other types of ADC architectures, e.g., pipelined and multi-bit sigma delta [5–14]. Few applications of Flash ADCs are data acquisition, satellite communication, radar processing, sampling oscilloscopes and high-density disk drives.

A typical Flash ADC requires 2^{N-1} comparators for an "N" bit converter. The resistor ladder is formed by 2^N resistors, which generates reference voltages for the comparators. The reference voltage for each comparator is one least significant bit (LSB) less than the reference voltage for the comparator immediately above it. When the input voltage is higher than the reference voltage of the comparator, it will generate a "1," otherwise the comparator output is "0." If the analog input is in between 0.312 V and 2.5 V, then the comparators in 0 through 7 generate "1" and all the remaining comparators generate "0".

The comparators will generate a thermometer code of an input signal. It is called thermometer code encoding because it is similar to a mercury thermometer, where the mercury column always rises to the appropriate temperature and no mercury is present above that temperature. The thermometer code will then decode into a binary form by thermometer-to-binary decoder.

The comparators are typically a cascade of wideband and low-gain stages. They are low gain because at high frequencies, it is difficult to obtain both wide bandwidth and high gain. They are designed for low-voltage offset, such that the input offset of each comparator is smaller than an LSB of the ADC. Otherwise, the comparator's offset could falsely trip the comparator, resulting in a digital output code not representative of a thermometer code. A regenerative latch at each comparator output stores the result. The latch has a positive

feedback, so that the end state is forced to either a "1" or a "0".

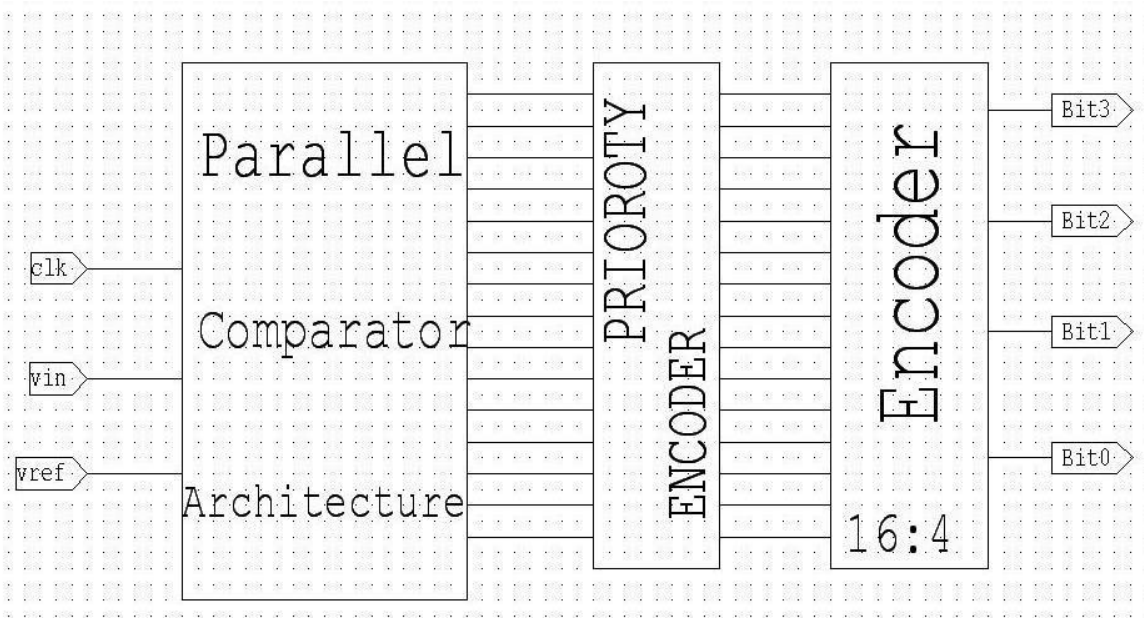

Fig. 16: *Schematic Architecture of 4-Bit Flash ADC.*

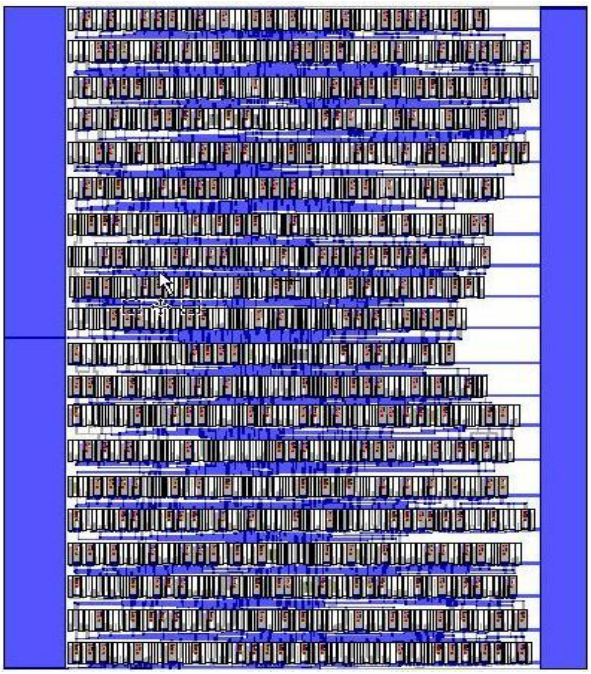

Fig. 17: *Core Layout of 4-Bit Flash ADC.*

Core Size = 1921 * 2589 μm, Core Area = 4973469 μm^2

After referring above equations to calculate these terms,

$NF = (SNR)_{inp}/(SNR)_{outp}$

$SNR = 20 \log(S_{max}/N_{max}) = 20 \log(2^N)$, $N_{max} < = 1$ LSB

$SNR = 20l\ n(2^4) = 20 * 1.386 = 27.725$ dB

Dynamic Range is the minimum to maximum output variation in the operational range.

DR = SNR

= 6.012 * N + 1.76, for N-bit ADC

DR = 6.012 * 4 + 1.76 = 25.80, for 4-bit ADC

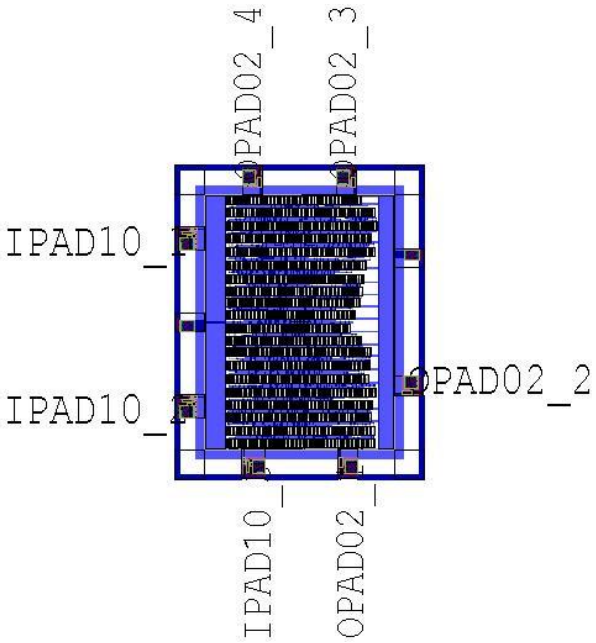

Fig. 18: *Chip Layout of 4-Bit Flash ADC.*

Chip Size = 2539.2 * 3207.2 μm, Chip Area = 8143722.24 μm^2

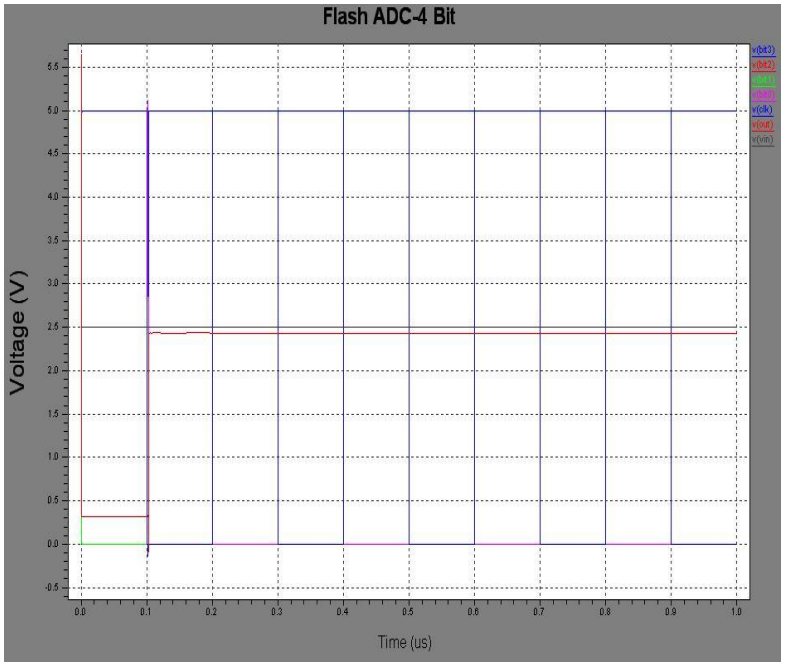

Fig. 19: *Simulation Result of 4-Bit Flash ADC.*

4.2. Parameters Calculated for 4-Bit Flash ADC

Clock Frequency = 66.7 MHz

Conversion time = 30 nsec

Differential Non Linearity (DNL) = 0.46 LSB

Integral Non Linearity (INL) = 0.82 LSB

Dynamic Range = 24 dB

Quantization Noise = 0.1 V

5. 8-BIT SUBRANGING ADC

It is based on the architecture of subranging ADC and uses above 4-bit Flash ADC and 4-bit DAC. Similarly, 12 and 16-bit architecture can be realized using 8 and 12 bit DACs.

N-bit DAC output is,

$$V_{out} = (b_{N-1} * 2^{N-1} + b_{N-2} * 2^{N-2} + \ldots\ldots + b_0) * V_{ref}/2^N \quad (25)$$

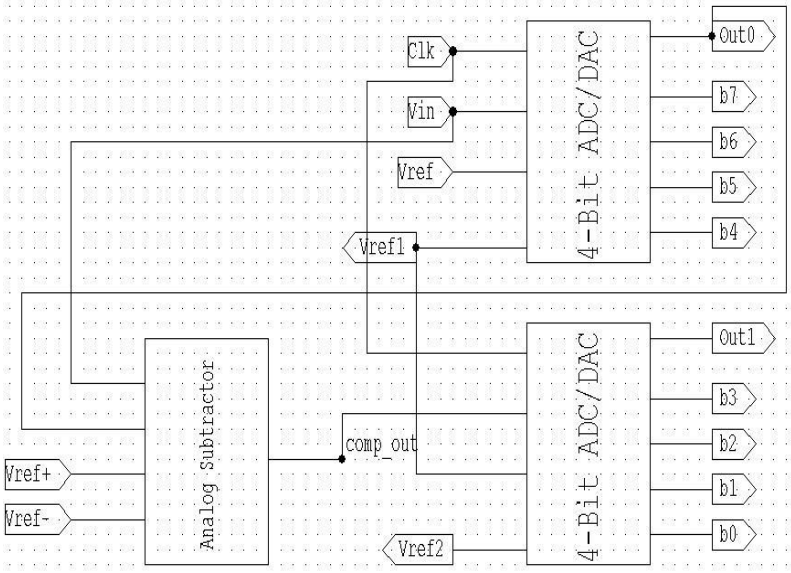

Fig. 20: *Schematic Architecture of 8-Bit Flash ADC.*

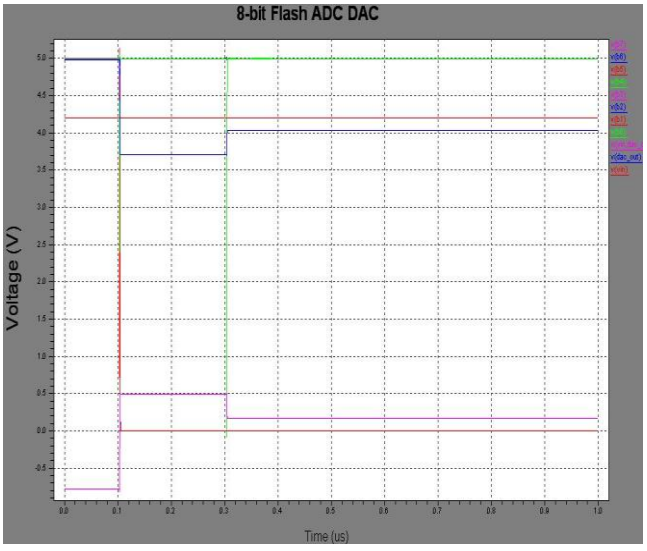

Fig. 21: *Simulation Result of 8-Bit Flash ADC.*

6. COMPARISON BETWEEN DIFFERENT TYPES OF ADCs

It is presented in Table III.

Table III:

ADC-Types	**Flash**	**SAR**	**Dual Slope**	**Pipeline**	**Sigma-Delta**
Conversion Method	**For n Bits, 2^{n-1} Comparators**	**Binary Search Algorithm**	**Analog Integration**	**Parallel Structure with Digital Correction Logic.**	**Over Sampling Modulator with Digital Decimation Filter**
Resolution (Bits)	Low 8	Medium 8–16	High 12–16	High 14	High 24
Power Consumption	High	Low	Low	Lower than Flash	Moderate
Speed	Very High	Medium	Low	High	Low-Medium
Limitations	Size and Power	Speed	a) Speed b) High precision external components required to achieve accuracy	a) Parallelism increases throughput at the expense of power and latency b) Chip Area	Higher order (4th order or higher) – multibit ADC and multibit feedback DAC.

7. CONCLUSIONS

Theoretical design for operational amplifiers, flash, subranging as well as other components were first carried out then spice simulations were done before preparing the full custom layout. Based on the operational amplifier, the designs for comparator, voltage subtractor, unity-gain buffer and closed loop amplifier were also done. Full custom designs for operational amplifier, comparator, 4-bit flash ADC and 8-bit subranging ADC were presented in this paper which is useful in picture/video signal quantization. Other higher subranging ADCs can be designed using 4-bit flash ADC similarly as 8/12 bit DAC components in the same way as presented in the design of 8-bit subranging ADC. Post layout extracted circuits' simulation was also carried out to verify its result with pre layout circuit simulation results using SPICE level 49 model parameters.

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