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Low Power RF QPSK MODEM Design

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ABSTRACT

System-level simulation including design of CMOS circuits for radio frequency QPSK MODEM targeting applications in 2.45 GHz industrial, scientific and medical (ISM) band has been presented in this paper. Based on the QPSK architecture, the MODEM consists of an analog mixer using a voltage multiplier, a 90 °phase shifter, delay circuits, a voltage adder and a filter to detect the information. A code reuse subsystem block consisting of Chebyshev filter type-II and lowpass RC filters is used prior to determine the envelope of the signal. The design will be useful in analog signal processing for its monolithic integration having higher speed and low cost. The MODEM circuit has been designed using SCL 1.2 µm CMOS foundry's model parameters. It can operate at a supply voltage of 3.5 V. The circuit consumes power less than 3.5 mW and analog mixer performs a conversion gain of + 9.54 dB (< 10 dB). Simulink system-level simulation verifies the stepwise behavioral aspects of the QPSK architecture and proves that its CMOS circuit's design presented in the paper shows similarity in the behavior with acceptable performance loss with respect to ideal case.

Keywords: *QPSK RF MODEM, analog CMOS circuit design, phase shifter, envelope detector, filter*

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1. INTRODUCTION

The 2.4 GHz industrial, scientific and medical (ISM) radio band technology has gained much interest during the last few years as a potential candidate for future wireless short-range data communication [1, 15]. In this paper, the design is focused on near-2.45 GHz ISM band. Due to its large bandwidth, ISMB has the advantage of high data rates.

In order to improve spectral efficiency and information capacity, phase modulation techniques such as BPSK or QPSK are used. But the most commonly used modulation scheme for wireless and cellular systems is quadrature phase shift keying (QPSK). Because QPSK involves phase-only modulation and provides a good balance between information capacity and ease of implementation, it does not suffer from BER degradation while the bandwidth efficiency is increased. Moreover, QPSK modulation permits twice the amount of information to be carried within the same bandwidth as BPSK with little additional complexity and thus is used in ISM bands.

This paper presents system-level design with simulation results of RF QPSK MODEM for 2.45 GHz band for wireless application. The circuit presented in this paper proves to be simpler and superior monolithic implementation for cost, performance comparison, power consumption and speed in its frequency range. In place of mixers, a singly balanced cascoded N and P channel Gilbert cell topology was used which takes

advantage of excellent current reuse; however, the use of P-channel devices limits the frequency of operation [3]. The system is suitable for both up and down-conversion operations [2].

The most noticeable feature presented in this paper has the reported frequency of operation (2.45 GHz) and the noise figure less than 10 dB for CMOS silicon technology-based mixer. Active CMOS devices limit the power consumption of the designed modulator to be less than 3.5 mW which proves the absence of high power consumption. It can operate at a supply voltage of 3.5 V, making it suitable for battery-operated system applicable to portable systems.

2. QPSK MODEM

The QPSK receiver architecture is shown in Figure 1. QPSK MODEM is a device which modulates as well as demodulates the baseband signal over the carrier; it is a part of QPSK transceiver.

This receiver consists of two coherent detectors supplied with the same input signal, namely, the incoming DSB-SC wave A_c $[1 + K_a\cos(\omega_s t)]\sin(\omega_c t)]$ with individual local oscillator signal that is in phase and quadrature phase with respect to each other. The frequency of the local oscillator adjusted to be the same as the carrier frequency f_c. The detector in the upper path is referred to be in phase-coherent detector for I-channel and another in the lower path is referred to as quadrature phase-coherent detector for Q-channel. These two detectors are coupled together to form negative feedback system. The system is designed in such a way as to maintain the local oscillator synchronous with the carrier wave [6].

In the transmitted reference scheme, two pulses per symbol are sent with a certain chosen delay [4, 5] between them. The modulated signal in both I and Q paths are delayed by 45° after its first multiplier then it further becomes the input to the second multiplier. To obtain the demodulated signal, both second multipliers' outputs in I and Q paths are added by a CMOS adder circuit and applied to the envelope detector as seen in Figure 1 [7].

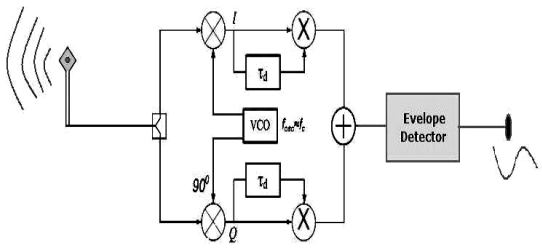

Fig. 1: *QPSK Demodulator (Receiver) Architecture.*

On mixing of modulated baseband cosine signal on carrier with the carrier of same frequency range of receiver and following the same analysis as applicable in Figure 1, a modulated signal is obtained after adder and baseband signal is recovered after the envelope detector.

3. SYSTEM-LEVEL MODELING OF RF MODEM

To determine the functional behavior of the proposed architecture, the above QPSK MODEM block is solved in system-level domain as described in Figure 2a. Here the same system analysis is followed assuming different filters. To understand the operation of this MODEM, a 2.45 GHz local oscillator signal is in phase with carrier wave used to generate the incoming DSB-SC signal. Under this condition, the I-channel output contains the desired demodulated signal m(t), whereas the Q-channel output is zero due to the quadrature null effect of the Q-channel. If the local oscillator phase drifts from its proper value by a small angle ø ° then there will be some signal appearing at the Q-channel output, which is proportional to the sinø that is ø for small ø. Now the Q-channel output will have the same polarity of the I-channel output for one direction of local oscillator phase drift and opposite polarity for the opposite direction of local oscillator phase drift, in this way, reducing phase error and combining I and Q channel output through adder which is connected to envelope detector.

The envelope detector block is shown in Figure 2b. It contains of a diode as a switch and Chebyshev lowpass filter type 2 which are connected in series. The diode acts as a rectifier. The Chebyshev lowpass filter specification is as follows:

Filter order: 4

Stop band frequency: 2.8 GHz;

Stop band attenuation: 60 dB

3.1. Time Domain Analysis

Since ISM band systems rely on timing information, a time-domain analysis [7,8] is explained in this paper. A conventional AM wave can be represented by,

$$S_m(t) = A_c[1 + K_a\cos(\omega_s t)]\cos(\omega_c t) \quad (1)$$

where $m(t) = A_s\cos(\omega_s t)$, $v_c(t) = A_c\cos(\omega_c t)$ and $K_a = A_s/A_c$, represent base band and career signals. A_c is the carrier amplitude and ω_c is the carrier frequency. This description is commonly used for carrier-based signals but can also be applied to pulse-based signals as long as they have a band-pass spectrum.

Now, consider the situation where two pulses of equal sign are transmitted. For the moment, assume only the upper path of the circuit shown in Figure 1. This path is denoted here as in-phase path. After multiplying the modulated signal with carrier, the signal for the upper path of the product1 is represented as,

$$I = S_m(t)*(A_c\cos(\omega_c t + ø(t))) \quad (2)$$

where ø(t) is the phase modulation, denoted by "0" for in-phase signals.

After calculating Eq. (2), we get

$$I = ½A_c^2[1 + \cos(2\omega_c t) + K_a\cos(\omega_s t) + ½K_a\{\cos(2\omega_c + \omega_s)t + \cos(2\omega_c - \omega_s)t\}] \quad (3)$$

or

$$I = ½A_c^2[1 - \cos(2\omega_c t) + K_a\cos(\omega_s t) - ½K_a\{\cos(2\omega_c + \omega_s)t + \cos(2\omega_c - \omega_s)t\}] \text{ for } v_c(t) = A_c\sin(\omega_c t). \quad (4)$$

After delaying this pulse in [6], the delayed path:

$$I_d = \tfrac{1}{2}A_c^2[1 + \cos(2\omega_c(t-\tau_d)) + K_a\cos(\omega_s(t-\tau_d)) + \tfrac{1}{2}K_a\{\cos(2\omega_c + \omega_s)(t-\tau_d) + \cos(2\omega_c-\omega_s)(t-\tau_d)\}] \quad (5)$$

To ease the analysis, a change of variable is made by letting $t' = (t-\tau_d)$

$$I_d = \tfrac{1}{2}A_c^2[1 + \cos(2\omega_c t') + K_a\cos(\omega_s t') + \tfrac{1}{2}K_a\{\cos(2\omega_c + \omega_s)t' + \cos(2\omega_c-\omega_s)t'\}] \quad (6)$$

This is the signal in the delayed path before the multiplier.

After multiplying the signals in the delayed path and original path in the second multiplier, it may be written as,

$$\text{I Channel path signal} = I*I_d \quad (7)$$

The previous analysis assumed perfect synchronization between the oscillator and the "pulse carrier." In reality, this is not the case. Unless the oscillator is being locked onto the incoming signal there is always a relative phase between the oscillator and the pulse carrier, denoting this relative phase as $\phi(t) = \pi/2$. This means that quadrature path $\omega_c t$ has to be replaced by $\omega_c t + \phi(t)$, and Eq. (2) can be written as

$$Q = S_m(t)*(A_c\cos(\omega_c t + \phi(t))) \quad (8)$$

Following the same analysis of the upper path, it can be expressed that the signal before adder in Q-path would be:

$$Q = \tfrac{1}{2}A_c^2[\sin(2\omega_c t) + \tfrac{1}{2}K_a[\sin(2\omega_c + \omega_s)t + \sin(2\omega_c - \omega_s)t]] \quad (9)$$

If ($\omega_c = \omega_m$) this means that after envelope detection, the result depends on "ø(t)." The output can even be zero whereas a positive value was expected. This is a well-known phenomenon in coherent detection. In coherent detection, the oscillator can be locked to the carrier but since in this situation there is a suppressed very weak carrier that is only present when the pulse is present and there is also narrowband interference, this is not possible. A possible solution is to add a similar path but now mixed with a sine (90-phase shift) instead of a cosine and adds the outputs after multiplied with the delayed path, resulting in the architecture shown in Figure 2a. This lower path is called the quadrature path. For the quadrature path, the signal after multiplication with the delayed path signal can be written as,

$$\text{Q Channel path signal} = Q*Q_d \quad (10)$$

3.2. Envelope Detection by Chebyshev Filter Type-II

Chebyshev filter type-II is used as an envelope detector in the code reuse subsystem block in MODEM system Simulink model. Since response of the Chebyshev filter is sharper than that of a Butterworth filter, it shows fewer ripples over the bandwidth, having a steeper roll-off and stopband ripple than does a Butterworth filter. Chebyshev filters have the property of minimizing error between the idealized and the actual filter characteristics but with ripples in the passband. The gain response as a function of angular frequency ω of the *n*th order lowpass filter is,

$$G_n(\omega,\omega_o) = 1/\sqrt{[1 + 1/\{\varepsilon^2 T_n^2(\omega/\omega_o)\}]}$$

In the stop band, the Chebyshev polynomial will oscillate between 0 and 1 so that the gain will oscillate between zero and $[1/(1 + \varepsilon^{-2})]$.

The smallest frequency at which this maximum is attained will be the cut-off frequency ω_o. The 3dB frequency f_H is related to f_c by [9], where $f_H = f_c/\cosh(n^{-1}\cosh^{-1}(1/\varepsilon))$. Its simulation results are shown in Figures 5a to 5e.

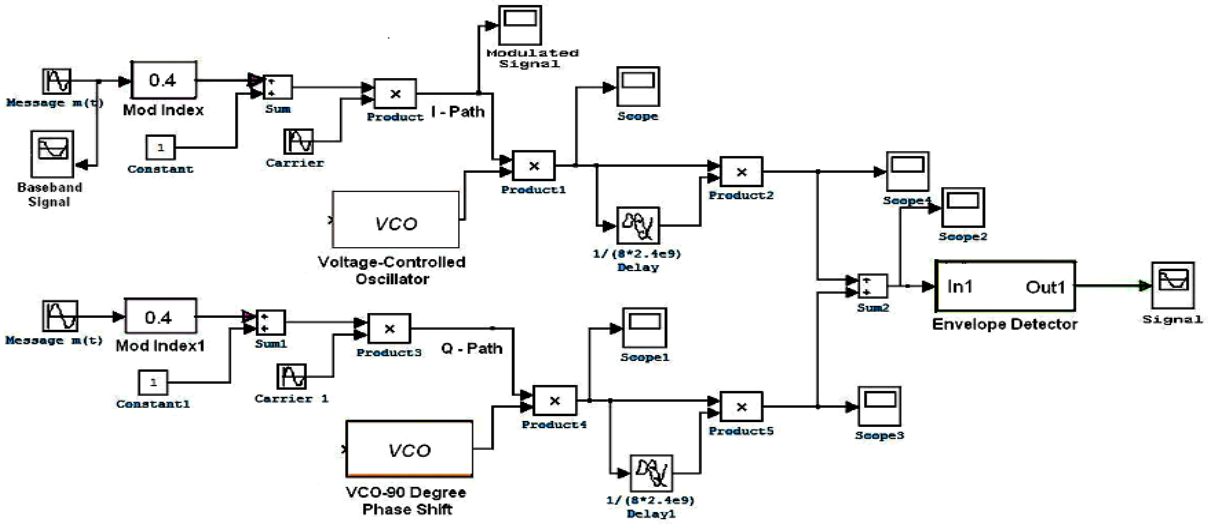

Fig. 2a: *QPSK MODEM System implemented in Simulink.*

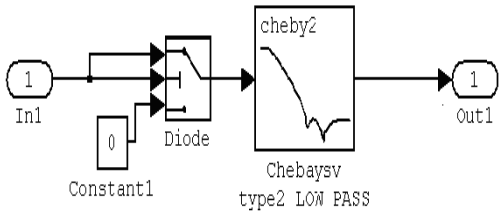

Fig. 2b: *Envelope Detector.*

4. CMOS QPSK MODEM DESIGN

In general, a cost-effective design is achieved by minimizing the number of external components for the MODEM IC and by using baseline IC process technology. The purpose of this paper is to present the design at circuit level for low-cost CMOS QPSK MODEM chip for its monolithic integration with rest of the hardware used in wireless communication application. In case of using foundries providing CMOS process, designers can implement low-loss signal line using thick metal and this enables RF blocks to have excellent performance (noise, linearity, etc.).

The circuit schematic of the proposed RF QPSK MODEM designed with an analog mixer (modulator), delay blocks, multipliers, and adder with envelope detector is shown in Figures 3a and b.

4.1. Analog Mixer

This paper describes a 2.45 GHz active doubly balanced down converting mixer as shown in Figure 4a. In this design, for reduction of flicker noise and high-speed LO switching, the resistive load and n-type MOS transistors (M4, M5, M6 and M7) are used respectively. Also,

to decrease the power dissipation, the size and gate bias of transconductance stage transistors (M3, M2) are the same. The mixer has a reasonable conversion gain, good rejection at the RF and local oscillator (LO) ports and a fully differential structure [10].

The RF signal is applied to transistors M2 and M3 which perform a voltage-to-current conversion. For correct operation, these devices should not be driven into saturation and, therefore, signals considerably less than 1 dB compression point should be used. Performance can be improved by adding degeneration resistors on the source terminals of M2 and M3. MOSFETs M4 to M7 form a multiplication function, multiplying the linear RF signal current from M2 and M3 with the LO signal applied across M4 to M7 which provide the switching function.

M2 and M3 provide +/− RF signal current and M4 and M5 switch between them to provide the RF signal or the inverted RF signal to the left hand load. M6 and M7 switch between them for the right hand load. The two P-type loads M8 and M9 form a current-to-voltage transformation giving differential output IF signals.

4.2. Mathematical Behavior of Analog Mixer

The proposed CMOS mixer is shown in Figure 4a. It is based on bias feedback technique [11]. The drain current I_d of an NMOS transistor in the saturation and triode regions can be expressed as,

$$I_d = \tfrac{1}{2}\mu C_{ox} W/L(V_{gs}-V_t)^2 = K(V_{gs}-V_t)^2 \quad (11)$$

$$I_d = 2K[(V_{gs}-V_t)V_{ds}-\tfrac{1}{2}V_{ds}^2] \quad (12)$$

where I_d is the drain current, μ is the carrier mobility constant, C_{ox} is the oxide capacitance, W is the device geometrical width, L is the length, V_t is the threshold voltage, V_{gs} and V_{ds} are the gate-to-source voltage and drain-to-source voltage respectively. The term, $K = \tfrac{1}{2}\mu C_{ox} W/L$ is known as the transconductance parameter. The differential current, can be mentioned as [12] and [13].

$$I_{out} = 2\sqrt{2K V_{RF} V_{LO}} \quad (13)$$

4.3. I/Q Path of the MODEM

The mathematical and theoretical operations of both I and Q channels are mentioned in this paper. This section includes only circuit design description. To determine the accuracy of the result, here some modifications are required as compared with the system-level modeling. The modified blocks of both I and Q paths are presented in Figure 3b. The typical values of RF and LO amplitude voltages are taken as ± 50 mV and ± 120 mV respectively.

4.3.1. I-Channel Path

Two multipliers and an RC delay circuit form the I-channel path. A 200 MHz signal-based DSB-SC modulated wave is mixed with a carrier of 2.45 GHz. This gives only higher frequency term after the first multiplier. To

overcome the problem of interfacing, an MOS diode is connected after the first multiplier. This signal is 45 ° delayed by RC delay network, after multiplying delay and no-delay path signals, it gives the output of I-channel path.

4.3.2. Q-Channel Path

In Q-channel only a phase shifter is extra, others are same as in I-channel. The phase shifter changes the incoming signal phase by 90 ° originated from the VCO. This paper presents MOS transistor-based phase shifters, has been realized only from two RC networks connected in series as shown in Figure 4c. One RC network gives 45° phase shift.

4.4. CMOS Adder

In this paper, a modified version of simple differential pair CMOS voltage adder is presented. In the common-drain configuration, it is used to perform two-input voltage addition; the circuit is shown in Figure 4b. The common-drain configuration makes the circuit capable of operating at high frequencies [14,15]. A complete circuit analysis is performed assuming that all transistors are identical and input signals V_x and V_y are balanced differential voltages [16]. According to KCL theory, it may be written as

$$V_x - V_y = (V_1\ V_2)/2 \quad (14)$$

For n input, it may be written as

$$V_x - V_y = (V_1 + V_2 + \ldots V_n)/n \quad (15)$$

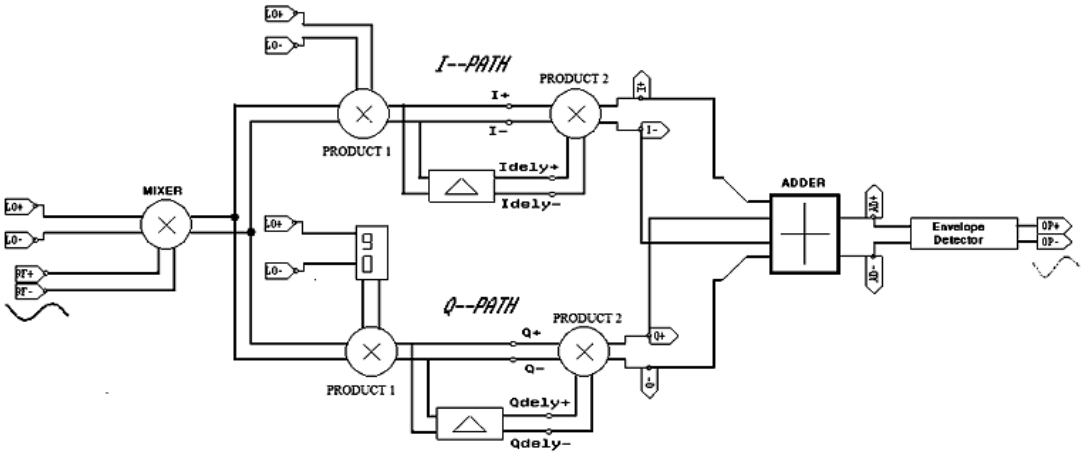

Fig. 3a: *Proposed QPSK Architecture for Circuit-Level Implementation.*

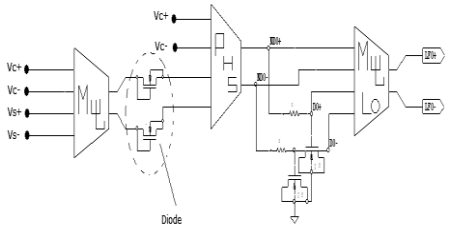

Fig. 3b: *Schematic of I/Q Path.Module wise Circuits are Presented Here.*

Table I:*Specifications of various Parameters.*

Parameter	**Specification**
Supply voltage	3.5 V
Base band signal	200 MHz
Carrier	2.45 GHz
W	> 10 µm
L	1.2 µm
Conversion gain of Mixer (Up conversion)	9.54 dB
Power consumption	3.5 mW
Resistance	10 kΩ

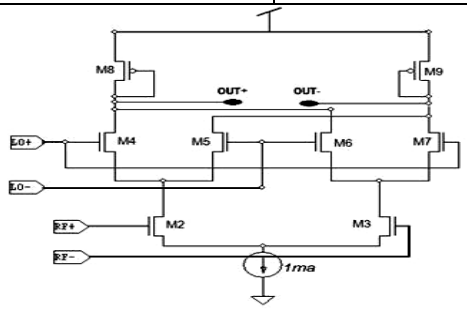

Fig. 4a: *Analogue Multiplier.*

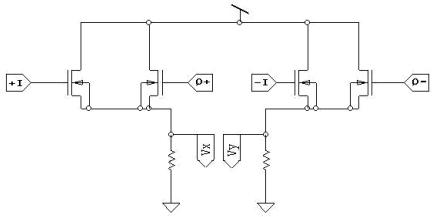

Fig. 4b: *Differential CMOS Adder.*

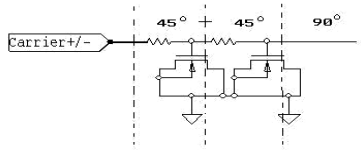

Fig. 4c: *90 Degree Phase Shifter.*

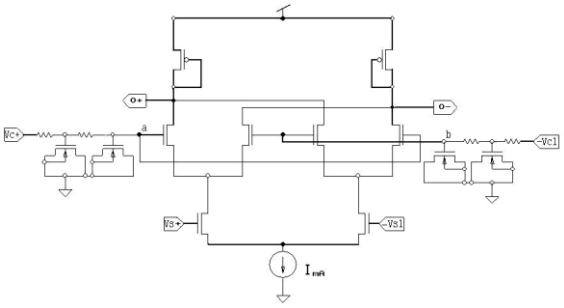

Fig. 4d: *Multiplier with 90 Degree Phase Shifter.*

Thus, by combining I and Q channel outputs in an adder circuit, as shown in Figure 3a, output is retrieved by using RC pair network.

5. SIMULINK AND SPICE SIMULATION RESULTS

To verify the functional behavior of the proposed QPSK MODEM, the system was first simulated in ideal situation. The initial phase of the oscillator was set to zero. The delay in the receiver matched the delay between the signals in the transmitter and the oscillator period was a perfect integer of this delay. No amplitude mismatch was present in the two paths and the oscillator signals had a perfect quadrature relation. Oscillator amplitude in both paths was set to one. The absolute value of the output in this ideal case serves as the reference value as from the mathematical analysis of MODEM, it followed that any amplitude and delay mismatch appearing in the system will degrade the output value. Figure 5 shows the simulation plot of the proposed architecture. The proposed output waveform contains no

negative term, so there is no chance of performance degradation of the system.

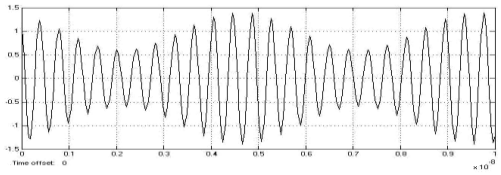

Fig. 5a: *Modulated Signal.*

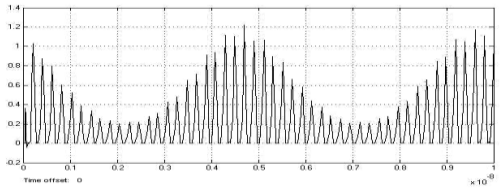

Fig. 5b: *Output of I-Path Product 2.*

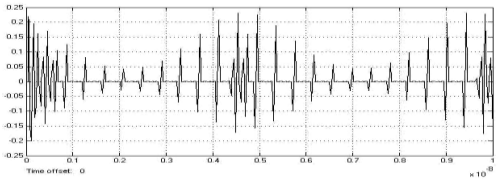

Fig. 5c: *Output of Q-Path Product 2.*

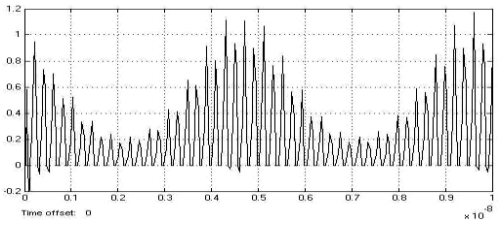

Fig. 5d: *Output of Adder.*

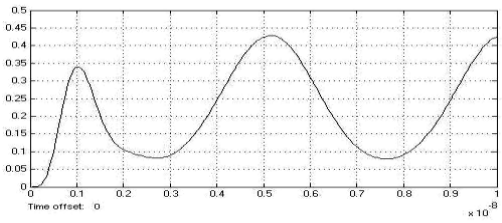

Fig. 5e: *Envelope of the Adder.*

All simulations were performed taking normalized amplitudes and to vary the simulation window from 0 to 10 ns during the whole design considering time offset as zero. Each submodule-wise simulation result was carried out using QPSK modeling in Simulink as shown in Figure 2a. It is presented step wise to show its functional behavior in detail. From Figures 5a to e, it is clear that no phase difference occurred at the output envelope compared with the baseband input.

The simulation results of QPSK MODEM shown in Figures 6a to e have been obtained from Spice simulation using its Hspice model parameters from 1.2 µm SCL CMOS technology. The specifications are known from Table I. All simulations were performed using 3.5 V supply voltage. The differential RF input cosine waves applied at the input terminals V_{RF} and V_{LO} of the circuit have an amplitude of ± 50 mV, ± 120 mV and frequencies of 200 MHz and 2.45 GHz respectively. ± 150mV waveform is obtained at output of the mixer. Figure 6a shows that the analog mixer output works as a source to produce modulated signal. There is no phase change displayed relating to input as seen in respective Figures. Figure 6e is the required output signal of the MODEM. This gives very less performance degradation compared to baseband input.

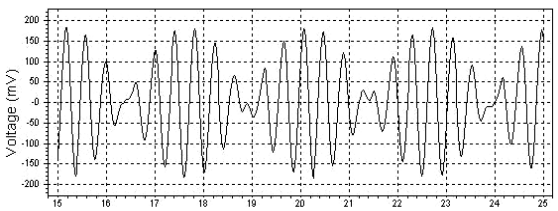

Fig. 6a: *Input to I/O Path (Modulator Output).*

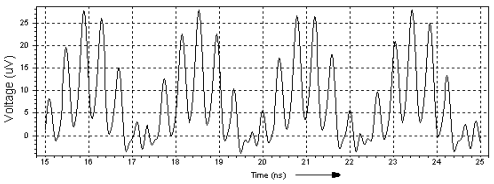

Fig. 6b: *Output of I Path Product 2.*

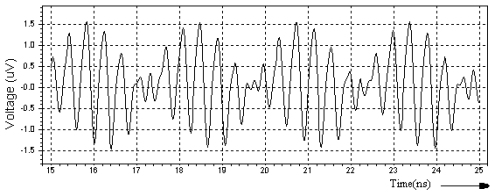

Fig. 6c: *Output of Q Path Product 2.*

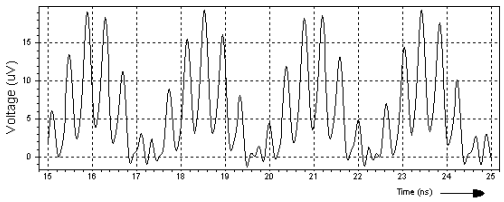

Fig. 6d: *Output of Adder.*

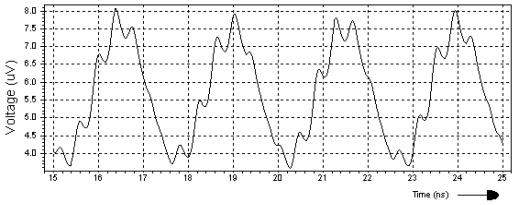

Fig. 6e: *Output of Envelope Detector.*

The magnitude of signals as function of time is shown in simulation results presented in Figures 6a to e. Due to transient analysis of initial set-up, SPICE simulation window varies from 15 ns to 25 ns, onward. It happens due to the initial-stage boundary condition setup. Comparing step-wise simulation results of Figures 5a to e with those of Figures 6a to e, it is clear that the proposed architecture behaves correctly.

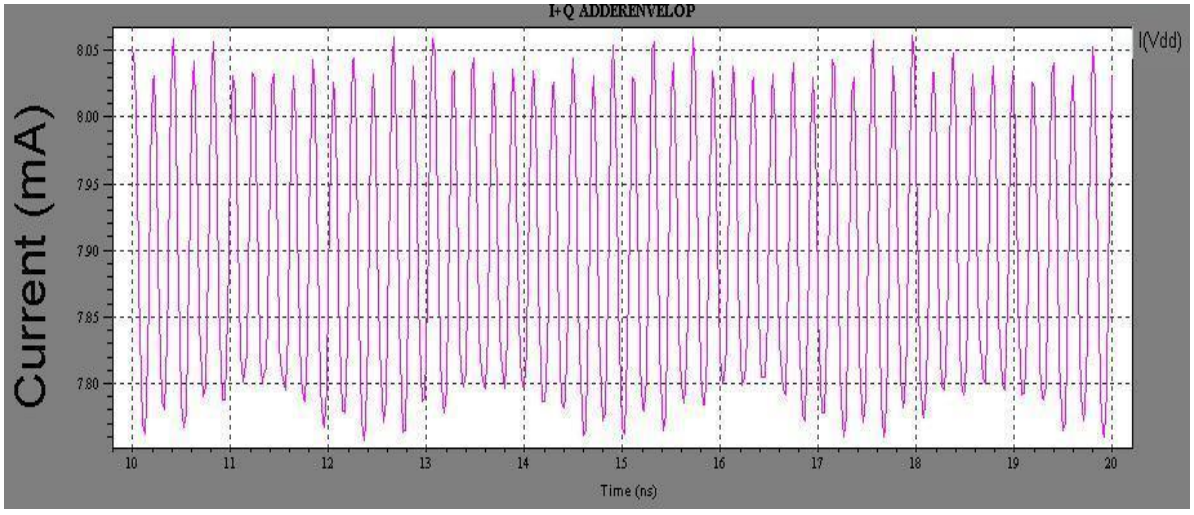

Fig. 7 *Power Supply Current*

From Figure 7, the current drawn through power supply (V_{dd}) shows that the bias current of the modem is 7.76mA and active output power is less than 3.5mW while total consumed power by the circuit including its dc biasing condition is 28.17mW. A comparison table has been presented for the power consumption of different makes of rf Modems as well as design presented in this paper, in Table 2.

Table II: *rf Modem Power Consumption*

Rf Modem Device Name	Frequency	Power/Supply Voltage
CC2500 Texas Instrument	2.4 GHz	93.85mW/3.9V
WHM900 - RF Modem Modules	900– 928 MHz	216mW/6V
9XCite RS-232/485 RF Modem	902–928 MHz	1.89W/7-18V
ZRT Radio Modem (ZRT169TR-1)	406–512MHz	750mW/12V
ZRT450TR-5	406–465MHz	5W/12V
XStream Digi International Part No: X24-019PKI-RA	2.4 GHz	50mW/7-18V
Paper Design	2.45 GHz	28.17mW(total)/3.5mW(active)/3.5V Sleep Current (7.76mA)

6. CONCLUSIONS

The architecture of CMOS, 2–2.8 GHz frequency band, RF QPSK MODEM as a part of transceiver is presented in the paper. System-level modeling with simulation in Simulink and its circuit design with SPICE simulation have been carried out and presented in the paper. Matlab code is also developed to verify these results. The simulation results, based on QPSK MODEM circuit implementation using trusted Hspice model parameters for the SCL 1.2 μm CMOS foundry, show better performances in terms of noise, bandwidth and input/output range. It is also a track record to prove its behavior at lowcast 1.2 μm CMOS technology at this frequency. The circuit can be operated at 3.5 V supply voltage with good simulation result. The circuit consumes less than 3.5 mW power and has good linearity. The absence of an envelope detector gives great advantage to the system, like reduced circuit complexity, smaller size, less power consumption, low cost, etc. Due to monolithic integration, low voltage and high-frequency operation makes the CMOS MODEM simpler.

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