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Low-Voltage Low-Power Single Supply Rail-to-Rail High Resolution Comparator in 0.18 µm CMOS Technology

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ABSTRACT

This paper presents an absolute input rail-to-rail ultrahigh-resolution comparator for low-voltage low-power applications. To enhance the input range rail-to-rail, the proposed comparator utilizes dynamic configuration with a MOSFET-only clock booster to supply a boosted voltage for pre-amplifier stage. Cadence SPICE simulations of the proposed comparator in a 0.18 µm CMOS process confirm the rail-to-rail input range with a supply voltage of 1.2 V with a decision time less than 9 ns. The dynamic power consumption of the proposed comparator is 59.3 µW with a clock frequency of 1 MHz.

Keywords: *Rail-to-rail, charge pump, dynamic compartor, non-overlap clock, low voltage*

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1. INTRODUCTION

Battery-powered applications such as medical monitoring and personal telemetry systems have major concern to ensure a long operation life for any instrument. Therefore, most circuit designers focus on low-voltage circuits to reduce the power consumption in the system. Typically, the threshold voltage of NMOS and PMOS devices restricts circuit to perform functionality up to rail-to-rail input signal range.

The comparator is an important element in signal processing systems, such as telecommunication interfaces, analog-to-digital converter as well as in sensory circuits [1]. The comparator contributes major part of power consumption in any analog-to-digital converter (ADC) system. Thus, design of a low-voltage low-power comparator is an important research area. Many low-voltage low-power comparators have been proposed [2]. Low power dissipation requirement in portable mobile communication and biomedical applications has encouraged research efforts in designing low-voltage analog circuits [3]. With low-voltage supply, it is very hard to achieve high resolution through a comparator unless it works for rail-to-rail operation.

In this paper, rail-to-rail comparator architecture is proposed for achieving ultrahigh resolution operating with low-voltage supply. Section II provides brief operation of conventional dynamic comparator. Section III describes proposed rail-to-rail comparator. In Sec. IV, results are summarized and conclusion is drawn in Section V.

2. DYNAMIC COMPARATOR

A dynamic comparator is shown in Figure 1 [3]. It consists of preamplifier as a differential input pair (M1, M2), a CMOS latch circuit, and an S-R latch. The CMOS latch is composed of an n-

channel flip-flop (M4, M5) with a pair of n-channel transfer gates (M8, M9) for strobing and an n-channel switch (Ml2) for resetting, and a p-channel flip-flop (M6, M7) with a pair of p-channel preamplifier transistors (M10, Ml1); clk1 and clk2 are the two non-overlapping clocks. The dynamic operation of this circuit is divided into a reset time interval and a regeneration time interval. During clk2, the comparator is in the reset mode. Current flows through the closed resetting switch M12, which forces the previous two logic state voltages to be equalized. After the input stage settles on its decision, a voltage proportional to the input voltage difference is established between nodes *a* and *b* in the end. This voltage will act as the initial imbalance for the regeneration phase.

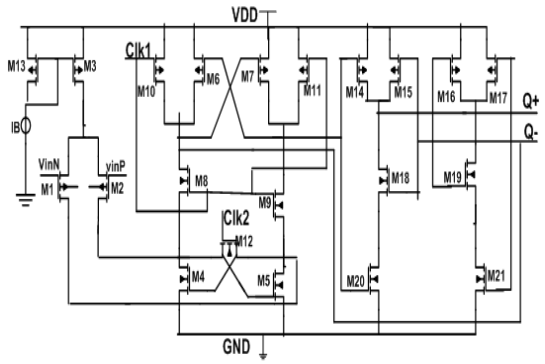

Fig. 1: *Conventional Dynamic Comparator.*

The regeneration is initialized by the opening of switch M12. Since the strobing transistors M8 and M9 isolate the n-channel flip-flop from the p-channel flip-flop when d is low, the use of two non-overlapping clocks performs the regenerative process in two steps. The first step of regeneration is within the short time slot between clk2 getting low and clk1 getting high. The second regeneration step starts when clk1 gets high and M8 and M9 are closed. The following *S-R* latch is driven to full complementary digital output levels at the end of the regenerative mode and remains in the previous state in the reset mode. The input common mode range for PMOS differential amplifier is given by [4]:

$$V_{IC(max)} = V_{DD} - V_{DSsat3} - V_{GS1} \quad (1)$$

$$V_{IC(min)} = V_{DS4} + V_{DSsat1} - V_{GS1} \quad (2)$$

Saturation condition for PMOS (M1) transistor

$V_{GS1} - |V_{TP1}| = V_{DSsat1}$

Or $- |V_{TP1}| = V_{DSsat1} - V_{GS1}$

Putting $(V_{DSsat1} - V_{GS1})$ value in Eq. (2)

$$V_{IC(min)} = V_{DS4} - |V_{TP1}| \quad (3)$$

It can be stated from Eq. (3) that if $V_{DS4} = |V_{TP1}|$, the value of $V_{IC(min)}$ can go down up to the ground rail value. Equation (1) shows that $V_{IC(max)}$ cannot achieve supply rail (V_{DD}) value because of subtracted value by $(V_{DS3} + V_{SG1})$. Therefore, the above comparator cannot achieve rail-to-rail input common mode range (ICMR).

3. PROPOSED RAIL-TO-RAIL COMPARATOR

It is difficult to design a low-voltage rail-to-rail comparator using conventional V_T CMOS technology. Equation (1) shows that if V_{DD} value for input pair transistor is higher than main V_{DD} supply, then we can achieve ICMR rail-to-rail for the comparator shown in Figure 1. For a single-supply circuit, it is not possible to provide second V_{DD} supply rail in the circuit; only a charge pump can generate higher voltage

value for a single-supply circuit. In the proposed comparator, we separate out input differential stage for supplying higher voltage than supply voltage V_{DD} using charge pump circuit proposed in [5]. The charge pump circuit used for generating boosted voltage value is shown in Figure 2. The boosted output voltage value depends upon the number. of stage and the capacitance value of the stage. The lumped capacitance of the charge pump circuit can degrade the output voltage value, and settling time of output voltage also depends upon lumped capacitance and the number of stage. For a suitable output voltage value, the optimization is needed iterative capacitance value with fixed number of stage. The proposed rail-to-rail comparator is shown in Figure 3 utilizing boosted supply voltage (V_{DD_CP}) for input differential stage. For the proposed comparator, the maximum input voltage value for comparison can be written by replacing V_{DD} value by V_{DD_CP} in Eq. (1).

$$V_{IC(max)} = V_{DD\_CP} - V_{DSsat3} - V_{GS1} \quad (4)$$

For $V_{IC(max)}$ to be V_{DD} the value of $V_{DD\text{-}CP}$ should be

$$V_{DD\_CP} = V_{DD} + V_{DSsat3} + V_{GS1} \quad (5)$$

Putting V_{DD_CP} value in Eq. (4)

$$V_{IC(max)} = V_{DD} \quad (6)$$

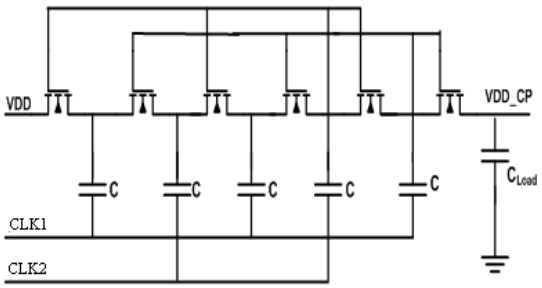

Fig. 2: *Charge Pump Circuit for Generating Boosted Supply Voltage.*

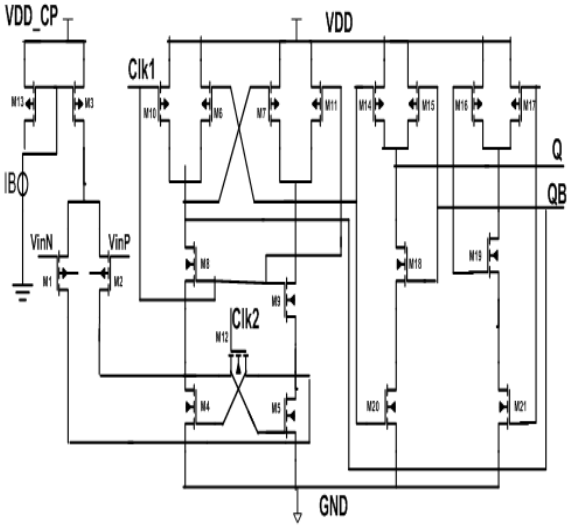

Fig. 3: *Purposed Input Common Mode Range Rail-To-Rail Comparator.*

4. SIMULATION RESULTS

Cadence virtuoso platform was used to design and simulate the proposed rail-to-rail comparator using UMC 0.18 μm CMOS process. From cadence virtuoso platform, virtuoso schematic editor, analog design environment (ADE) and spectre were utilized for schematic, different analysis and process corner simulation for the proposed comparator. Using spectre tool, the proposed comparator has been simulated in five different corners at room temperature, typical-typical, slow-slow, fast-fast, slow-fast, and fast-slow as shown in Figure 4. The proposed comparator is able to compare 5 μV signal at 100 KHz frequency shown in Figure 5.

The output of charge pump VDD_CP is also shown in Figure 5, which is used for power supply rail for differential input stages of the proposed comparator. For charge pump circuit,

the number. of stages is five and value of stage capacitance and load capacitance are taken as 1.5 pf and 10 pf respectively. Charge pump circuit is generating 1.7 V output voltage with 8 µs settling time. A 1.2 V ramp signal applied for duration of 40 µs with different reference levels to verify absolute input rail-to-rail operation is shown in Figure 6.

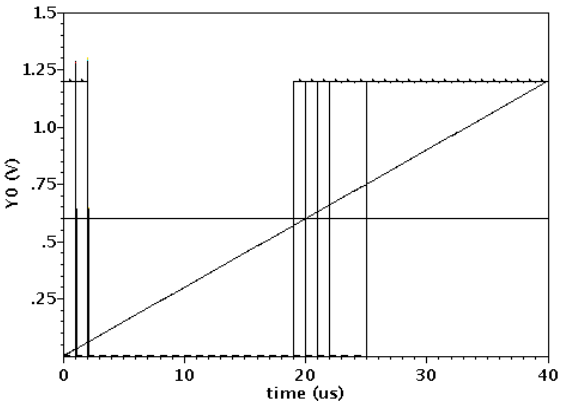

Fig. 4: *Process Corner Simulation Result Using Corner Simulation Tool from Cadence ADE.*

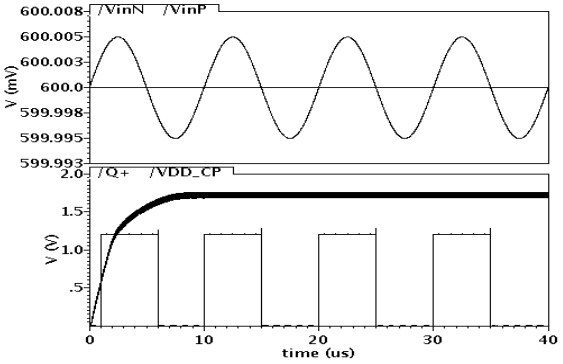

Fig. 5: *Transient Simulation Result of the Proposed Comparator.*

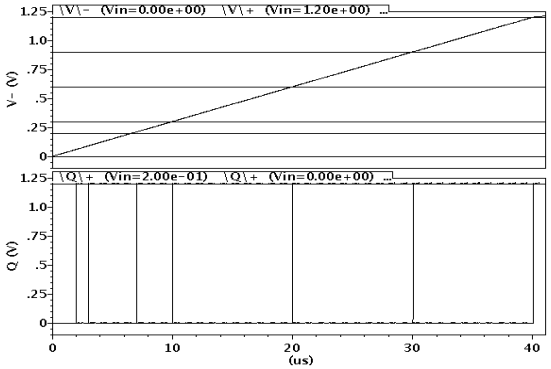

Fig. 6: *Simulation Result of the Proposed Comparator for Rail-to-Rail Input Common Mode Range.*

Table I: *Simulated Performance of the Proposed Comparator and Compared with Reported Studies.*

	Ref [3] 1992	**Ref [5] 2011**	**Ref [6] 2009**	**Ref [7] 2011**	**This Work**
Power supply	+ 2.5 V/−2 5V	1 V	1.8 V	0.8 V	1.2 V
Resolution	8 Bit	-	-	12 Bit	16 Bit
Decision time	3 ns	1 ns	1 ns	117 ns	< 9 ns
Clock frequency	65 MHz	40 MHz	-	15 MHz	1 MHz
Input operation range	–1.25 V–+ 1.25 V	0.25 V–0.75 V	0.225 V–1.2 V	0 V–0.5 V	0 V–1.2 V
Power dissipation	-	17 µW	-	191.2 nW	59.3 µW
Technology	1.5 µm	0.13 µm	-	65 nm	0.18 µm

5. CONCLUSIONS

In this paper, a low-voltage low-power input common mode range rail-to-rail comparator is presented using charge-pump technique to enhance the input common mode range. Cadence spectre simulations of the proposed comparator in a 0.18 μm CMOS process confirm the rail-to-rail input range of the comparator with a supply voltage of 1.2 V and a dynamic power dissipation of 59.3 μW with a clock frequency of 1 MHz and a decision time of less than 9 ns.

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REFERENCES

1. V. Katyal, R. L. Geiger and D. J. Chen *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*. Dec. 2006. 5–8p.
2. S. M. Lee, T. Song, C. Cho, et al. *International Symposium on Signals, Circuits and Systems*. Sept. 2003. 2. 377–380p.
3. G. M. Yin, F. Op't Eynde and W. Sansen. *IEEE Journal of Solid- State Circuits.* Feb. 1992. 27(2).
4. 4. K. R. Laker and W. M. C. Sansen. *Design of Analog Integrated Circuits and Systems.* McGraw-Hill International Edn. 1994.
5. J. Zhou, R. M. Ziazadah, H. –H Ng, et al. *ISLPED-97*. Aug. 1997. 108–109p.
6. M. Hashemi, M. Sharifkhani, and S. M. Atarodi. *6th International Symposium on Electronic Design, Test and Application*. 2011. 195–198p.
7. S. M. Lee, T. Song, C. Cho, et al. *Electronics Letters*. July 2009. 45(14).
8. S. Lan, C. Yuan, Yvonne Y. H. Lam, et al. *54th International Midwest Symposium on Circuits and Systems*. Sept. 2011. 23. 1–4p.