Journal of VLSI Design Tools and Technology
Volume 2, Issue (1-3), Compilation 2012

STM JOURNALS

Power Reduction at 90 nm through Circuit Level Modification

Angshuman Chakraborty**, Sambhu Nath Pradhan
Department of ECE, N. I. T., Agartala, India

ABSTRACT

Along with dynamic power, leakage power has turned out to be a major contributor to the overall power consumption in VLSI circuits. This problem is even more stringent in nano-scale dimension devices according to the International Technology Roadmap for Semiconductors (ITRS). As the technological advancements demand more function per device with a significant shrinking in device dimension, heat per unit area is also escalating at an elevated rate. This turns out into degradation of device material, viz., di-electric breakdown, altered component characteristics, etc. This demands additional cooling arrangements to keep the heat density to a minimal operational range. Due to increased power consumption, the battery power also gets drained at a rapid rate. This demands bulky power sources in miniature devices, which is a great hindrance in hand-held portable gadgets. Static power dissipation occurs in run time as well as in active mode of operation of the device. In this work, we have proposed a run time leakage current reduction technique for the CMOS logic circuit at 90 nm technology. As a basic building block, we have selected NAND (universal gate) as our point of focus. We have compared the leakage value of the proposed NAND gate with the leakage of the normal NAND gate. Maximum leakage saving has been obtained more than 90%. The technique is also well suited for the reduction of dynamic power. Simulation results show up to 63.6% in dynamic power saving with small area and delay overhead.

Keywords: *BSIM, CMOS, DIBL, glitching power, nano-scale*

****Author for Correspondence*** E-mail: ans_22@rediffmail.com, Sambhu.pradhan@gmail.com

1. INTRODUCTION

The urge to integrate more functions per unit area in order to make compact portable devices, shrinking of process parameters has been of utmost importance. But shrinking of process parameters invites unwanted and uncontrolled leakage of current. These leakages are inversely proportional to the device dimension. Lower is the technology, more is the leakage. The leakage currents contribute to the majority of power consumption in nano-scaled devices. It can be as large as 50% contributor of the total power consumption. In VLSI regime, Total Power = (P_{STATIC} + $P_{DYNAMIC}$). Static power takes place whenever the device is in stand-by condition. Reverse biased P-N junction leakage, gate oxide tunneling, DIBL, hot carrier injection, and sub-threshold leakage are considered to be the major part of static leakage. Switching, glitching and short circuit power dissipation are the three major constituents of dynamic leakage. Many techniques have been evolved to deal with these leakage mechanisms. To name some of the leakage control techniques, dynamic threshold CMOS (DTCMOS) [2], body-biasing such as CMOS (VTCMOS), leakage control using multi-threshold design approaches [3–6], dual-threshold assignment [7, 8] etc., are the few of them. Run time leakage minimization

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through minimum leakage vector (MLV) has been discussed in [9–13]. But all the above mentioned techniques come with an additional overhead of increased transistor count and hence the delay. In our technique, we have come out with a simple idea which ensures saving of static as well as dynamic power in nano-scale regime. In the present case, we have considered NAD gate

A. *Normal CMOS NAND Gate*

We have considered NAND gate as a reference because of its universal nature. Any advantageous modification in the said gate design will result in a subsequent superiority for other designs. The referenced gate has been evaluated in terms of both pre- and post-layout simulations. The schematic, pre-layout o/p waveform, layout and corresponding waveform have been shown in Figures 1–4, respectively.

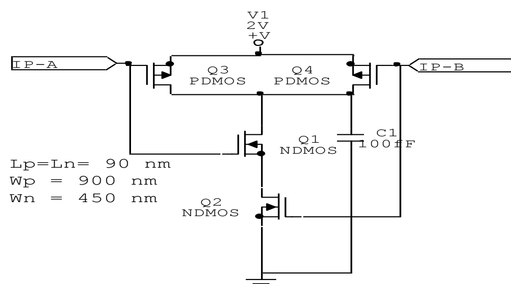

Fig. 1: *Normal 2-Input CMOS NAND Gate.*

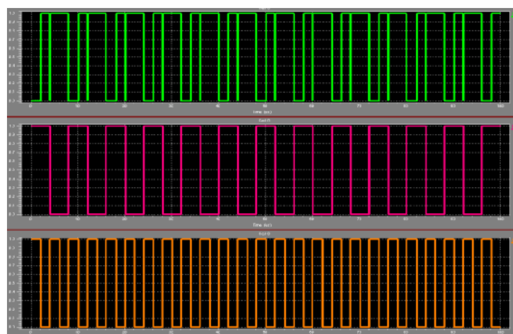

Fig. 2: *Pre-Layout Waveforms of Normal CMOS NAND Gate.*

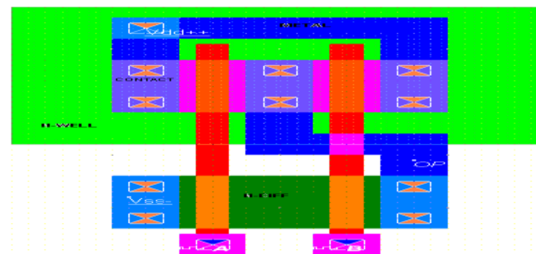

Fig. 3: *CMOS NAND Layout.*

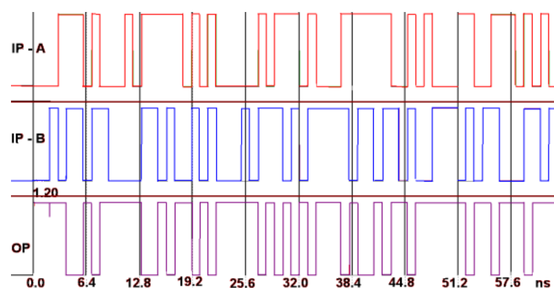

Fig. 4: *Post-Layout Waveforms of Normal CMOS NAND Gate.*

B. *Proposed CMOS NAND Gate*

In the newly modified proposed CMOS NAND gate, we have aimed at the reduction of its power dissipation. In the modified structure, we have added three new components (one capacitor and two n-channel enhancement type MOS transistors). The proposed circuit diagram for CMOS NAND is shown in Figure 5. The added section to the existing normal CMOS NAND gate has been highlighted in Figure 5. In the modified circuit, we have added one capacitor in the series path from V_{DD} to ground. As capacitor opposes DC current, it will block majority of static leakage from V_{DD} to G_{nd}. This is because, though there is minimal leakage, but it is sufficient enough to charge the capacitor to V_{DD} with a time constant set by the circuit parameters itself. There is no path for the capacitor to discharge and which will

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pull high the output for every combination of input. To overcome this problem, a combination of two NMOS transistors (Q5 and Q6) connected in series with each other has been placed in parallel path in between positive and negative terminal of the capacitor. Whenever the input A = 1 and B = 1, both the NMOS will be driven into saturation, providing a low-resistance path for the capacitor to discharge and to pull down the output from 1 to 0. Thus, the overall functionality of the CMOS NAND gate is retained. The value of the capacitor has to be chosen in such a manner that it will block the desired frequency. In the present case, we have selected the value of the capacitor as 100 fF. This extra capacitance increases the area and decreases the speed of 2-input NAND. The single modified section shown in Figure 5 can be shared by several logic gates (Figure 9) in the circuit. In that case, the area increase compared to the original circuit is very nominal. Instead of using two extra transistors, single transistor can also serve the purpose but that requires judicious choice of transistor dimensions and its capacitance value. Simulation at 90 nm technology shows that the delay for 50 fF and 100 fF is 10.3 ns and 10.8 ns, respectively.

2. EXPERIMENTAL RESULT

The experimental result that has been obtained is discussed and tabulated in this section. The power dissipation result of modified NAND gate has been compared with its normal counterpart.

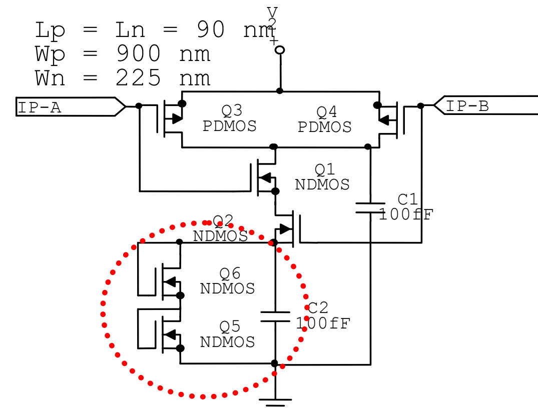

Fig. 5: *Proposed 2-input CMOS NAND Gate.*

The result of the proposed circuit shows a significant saving of power with the normal one. Tanner CAD Tool – V (14.1), with BSIM 3.1 and 90 nm PTM model – has been used for simulating the research idea. The length of all the transistors was taken to be 90 nm and width of PMOS as 900 nm and width of NMOS as 450 nm. Output load was taken to be capacitive of 100 fF. Figures 6, 7 and 8 are the pre-layout waveforms, layout and post layout input-output waveforms of the proposed NAND gate respectively. In Figures 6 and 8, IP-A, IP-B are the input and output of proposed NAND gate respectively. From the Figures, it is observed that the output waveform generated during the simulation of the new proposed NAND gate shows almost no discrepancies with the normal expected behavior of NAND gate. Thus the newly proposed NAND gate yields a good agreement with the reported results of proposed NAND gate. The simulation result also confirms that the proposed NAND gate designed in nano-scale regime operates correctly over a frequency range of KHz to

GHz. Power dissipation result has been presented in the following section.

To get the runtime leakage power, normal 2-input NAND and proposed NAND gate have been simulated for all input combinations. The leakage power has been tabulated in Table I. The last column of Table I enumerates the leakage saving for each corresponding input combination. Maximum saving is 91.5% for the input combination A = 1, B = 0 and minimum saving is 9.33% for the input combination A = 0, B = 1. The average saving is 52.45% as shown at the last row of Table I. It may be noted that we have assumed that the input combination occurs independently and they have rail to rail swing. To find the effectiveness of total power dissipation of our proposed NAND gate in the normal mode of operation, we have simulated both the NAND gates after applying 100 random input combinations. The dissipation obtained after this simulation is total power (Table II) which has switching and leakage components. From Table II, it is seen that the proposed NAND gate dissipates 63.6% (MHz scale) less power compared to normal NAND gate. Delay comparison is given in Table III. Figures 10 and 11 represent the corresponding graph plot of the values tabulated in Tables I, II and III.

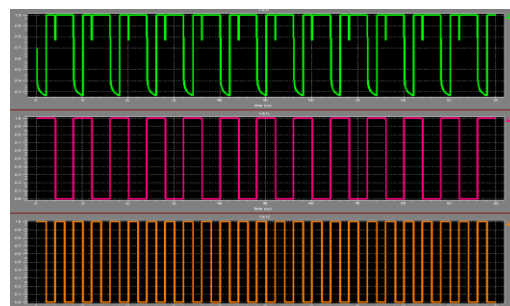

Fig. 6: *Pre-Layout Waveforms of Proposed CMOS NAND Gate.*

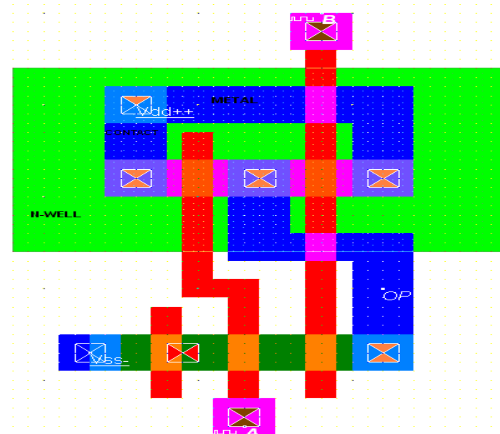

Fig. 7: *Proposed CMOS NAND Layout.*

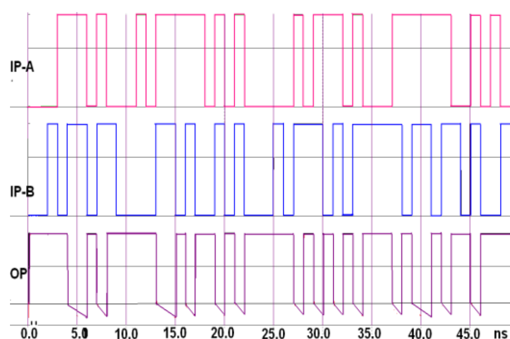

Fig. 8: *Post-Layout Waveforms of Proposed CMOS NAND Gate.*

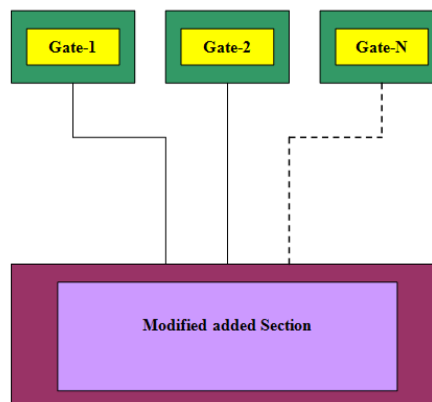

Fig. 9: *Sharing of Leakage Modification Section by Several Logic Gates.*

Table I: *Leakage Power Result.*

A	B	Pre-Layout Simulation			Post-Layout Simulation		
		Leakage Power Simple NAND (pW)	**Leakage Power proposed NAND (nW)**	**% Saving of Proposed NAND**	**Leakage Power Simple NAND (nW)**	**Leakage Power Proposed NAND (nW)**	**% Saving of proposed NAND**
0	0	358	792	21.58	1190	972	18.31
0	1	2.51	952	09.33	1230	1161	05.60
1	0	358	221	91.56	2750	310	88.72
1	1	2.51	205	87.34	1780	295	83.42
Average saving				52.45	Average saving		49.01

Table II: *Total Power Result.*

Power of Simulated NAND Gate in MHz Scale					
Pre Layout Simulation			**Post Layout Simulation**		
Simple NAND	**Proposed NAND**	**% Power Saving of Proposed NAND**	**Simple NAND**	**Proposed NAND**	**% Power Saving of Proposed NAND**
1600 nW	583 nW	63.6	2100 nW	866 nW	58.76

Table III: *Delay Comparison.*

Delay Comparison					
Pre-Layout			**Post-Layout**		
System	**Rise Time (ns)**	**Fall Time (ns)**	**System**	**Rise Time (ns)**	**Fall Time (ns)**
Normal NAND	37.325 nS	28.066 nS	Normal NAND	39.125	31.056
Proposed NAND	37.325 nS	38.657 nS	Modified NAND	39.125	39.085
Delay increases in Modified NAND gate by = 13.93%			Delay increases in Modified NAND gate by = 10.26%		

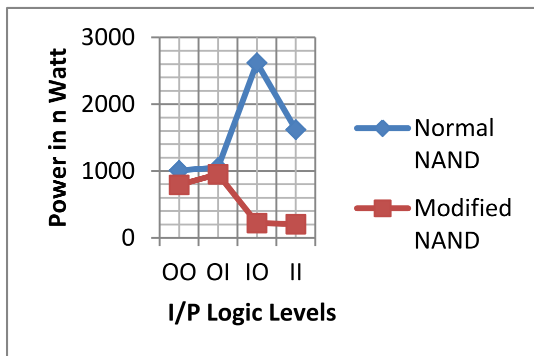

Fig.10: Pre-Layout Leakage Power Comparison.

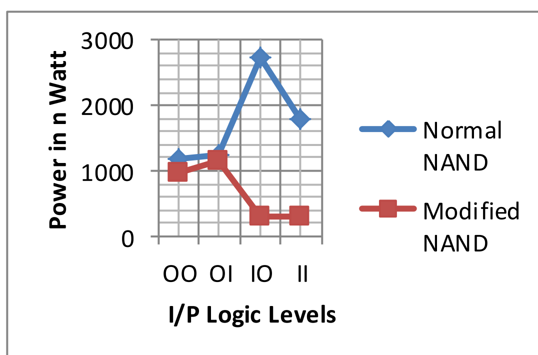

Fig. 11: Post-Layout Leakage Power Comparison.

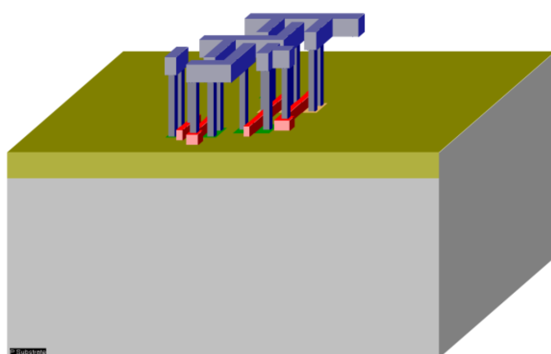

Fig.12: 3D View of the Layout of the Proposed CMOS NAND Gate.

4. CONCLUSIONS AND FUTURE SCOPE

In this paper, a new configuration of 2-input NAND gate has been presented. The modification has been made targeting lower leakage power dissipation. The modified configuration for CMOS NAND gate shows significant saving in power compared to conventional NAND gate. The modified configuration operates well in high frequency range. New NAND gate configuration exhibits total power saving. Modified configuration has overhead of one capacitor and two NMOS transistors. The new technique can be extended to NAND gate of any number of inputs. So, our future work target is extending this configuration to other logic gate of any number of inputs. The area impact due to this extra capacitance is to be studied in detail.

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