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Technology Limits on Differential Gain and Unity-gain Bandwidth of a Differential Amplifier: A Theoretical Analysis

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ABSTRACT

The limiting relationship between differential dc voltage gain and unity-gain bandwidth of an externally unloaded differential amplifier have been explored. It has been observed that the product of differential dc voltage gain and unity-gain bandwidth of a differential amplifier has an upper limit which is a technology constant.

Keywords: *Technology limits, differential amplifier*

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1. INTRODUCTION

There are some CAD tools available for the automatic synthesis of basic analog circuits, such as operational amplifiers, converters *etc*. for the given specifications. Often, users keep demanding more and more hard specifications for which the tool does not give a valid solution. A question always comes to the user's mind "Something is probably wrong with the tool?" Another question also comes to the mind "Whether the given specifications are practical at all or are they feasible in a particular (given) technology?"

The present study is an effort to answer the second question above. To explore the limits and limiting relationships, a circuit of current-mirror loaded differential amplifier has been chosen which is a commonly used first stage in various operational amplifiers and comparators. The two small signal parameters—*dc* differential voltage gain (Ad) and unity-gain bandwidth (UGB) have been considered for the current analysis. First, the analytical formulation was done and then the structures were simulated to verify the analytical results for seven different CMOS processes from varying fabrication houses in the range 1.25 μm down to 0.25 μm.

2. SMALL-SIGNAL RELATIONSHIPS OF A DIFFERENTIAL AMPLIFIER

The transistor level circuit for a current mirror loaded differential amplifier is shown in Figure 1.

A. Unity-Gain Bandwidth (UGB)

Unity-gain bandwidth (UGB) of the differential amplifier of Figure 1 is given by

$$UGB = \frac{g_{mi}}{2 \cdot \pi \cdot C_L} = \frac{1}{2 \cdot \pi \cdot C_L} \sqrt{\frac{k_n \cdot W_i \cdot I_o}{L_i}} \quad (1)$$

where g_{mi} is the transconductance of the input transistors M1 and M2, W_i is the width and length and L_i is the length of input transistors,

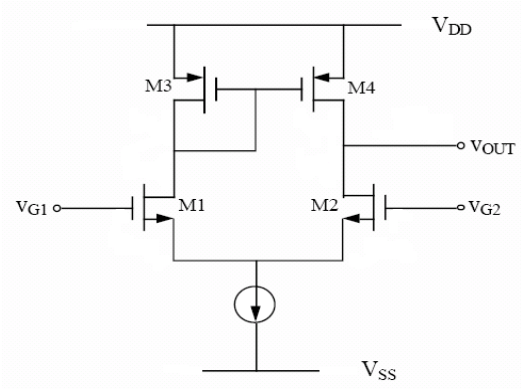

Fig. 1: *Differential Amplifier.*

k_n is the process trans-conductance parameter of input transistors (nMOS), and C_L is the total load capacitance (internal as well as external) at the output node.

B. Differential dc Voltage Gain (Ad)

The differential *dc* voltage gain (Ad) of the differential amplifier is given by

$$Ad = \frac{g_{mi}}{g_{di} + g_{dl}} = 2 \cdot \sqrt{\frac{k_n}{I_o} \cdot \left(\frac{W_i}{L_i}\right)} \cdot \left(\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_n\right)^{-1} \quad (2)$$

where I_o is the bias tail current of the differential amplifier, $g_{di}$and g_{dl} are the drain conductance of input and load transistors, respectively. The drain conductance g_d of a MOS transistor with length L and drain to source current as $I_o/2$ is approximated as

$$g_d = \frac{I_o}{2.L} \cdot \left(\frac{dx_d}{dV_{DS}}\right) \quad \ldots (3)$$

where $\left(\frac{dx_d}{dV_{DS}}\right)$ (known as channel-length modulation parameter) is a process parameter [1].

3. ANALYTICAL FORMULATION OF PRODUCT OF GAIN AND UNITY-GAIN BANDWIDTH

The product of the differential dc voltage gain and unity-gain bandwidth of a differential amplifier using Eqs. (1) and (2) can be written as

$$Ad * UGB = \frac{1}{2 \cdot \pi \cdot C_L} \sqrt{\frac{k_n \cdot W_i \cdot I_o}{L_i}} \cdot 2 \cdot \sqrt{\frac{k_n}{I_o} \cdot \left(\frac{W_i}{L_i}\right)} \cdot \left(\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_n\right)^{-1} \quad (4)$$

$$Ad * UGB = \frac{k_n}{\pi \cdot C_L} \cdot \frac{W_i}{L_i} \cdot \left(\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_n\right)^{-1} \quad (5)$$

Substituting the values of technology constants $\left(\frac{dx_d}{dV_{DS}}\right)$ as 0.1 μm/V for nMOS and 0.05 μm/V for pMOS transistors for 1.2 μm CMOS process in (5), it reduces to

$$Ad * UGB = \frac{10 k_n \cdot W_i}{\pi \cdot C_L} \cdot \left(1 + \frac{L_i}{2.L_l}\right)^{-1} \quad \ldots \quad (6)$$

This reduced expression can be obtained for other technologies by substituting the corresponding values of $\left(\frac{dx_d}{dV_{DS}}\right)$ for nMOS and pMOS transistors in Eq. (5).

4. COMPUTATION OF LOAD FOR AN UNLOADED AMPLIFIER

For an unloaded amplifier, the external capacitance is zero implying that the drain-to-

bulkcapacitances of the input and the load transistor form the capacitive load [2], *i.e.*

$$C_L = C_{L(\text{int})} = C_{dbi} + C_{dbl} \quad \ldots (7)$$

where C_{dbi} and C_{dbl} are the drain-to-bulk capacitances of the input and load transistors respectively.

For a transistor the drain-to-bulk capacitance is given by

$$C_{db} = C'_{db} + C_{d-sw} \quad \ldots (8)$$

where C'_{db} is bottom plate capacitance of the drain junction and C_{d-sw} is the side wall capacitance of the drain junction.

Further,

$$C'_{db} = A_d \cdot C_{jd} \quad \ldots (9)$$

A_d is the area of the bottom plate of the junction, which is the same as the drain area and C_{jd} is the junction capacitance per unit area for the one-sided step junction and is given by

$$C_{jd} = \frac{C_{j0}}{\sqrt{1+\frac{V_{DB}}{\phi_0}}} \quad \ldots (10)$$

where C_{j0} is the zero-bias junction capacitance and is a process constant given by

$$C_{j0} = \sqrt{\frac{qK_s\varepsilon_0 N_D}{2\phi_0}} \quad \ldots (11)$$

and V_{DB} is the drain-to-bulk potential of the junction. All other symbols have their usual meanings.

The built-in potential, ϕ_0 is given by

$$\phi_0 = V_T \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right). \quad \ldots (12)$$

where V_T is the thermal voltage, N_A and N_D are the doping densities of p-type and n-type materials on either side of the junction.

The sidewall capacitance of the drain region, C_{d-sw} is given by

$$C_{d-sw} = P_d \cdot C_{j-sw} \quad \ldots (13)$$

where P_d is the perimeter of the drain region excluding the portion/wall adjacent to the gate and

$$C_{j-sw} = \frac{C_{j\_sw0}}{\sqrt{1+\frac{V_{DB}}{\phi_0}}}. \quad \ldots (14)$$

Hence, the drain-to-bulk capacitance of a transistor can be written as

$$C_{db} = A_d \cdot C_{jd} + P_d \cdot C_{j-sw} \quad \ldots (15)$$

For the input transistor (n MOS type) we rewrite it as

$$C_{dbi} = (W_i * L_{d,n}) \cdot C_{jd,n} + (W_i + 2L_{d,n}) \cdot C_{j-sw,n} \quad \ldots (16)$$

and for load transistor (pMOS type)

$$C_{dbl} = (W_l * L_{d,p}) \cdot C_{jd,p} + (W_l + 2L_{d,p}) \cdot C_{j-sw,p} \quad \ldots (17)$$

where $L_{d,n}$ and $L_{d,p}$ are the lengths of drain extensions beyond the gate for n-type and p-type transistors respectively.

From equations (6), (15) and (16), the total load seen on the output node of the amplifier is given by

$$\begin{aligned} C_L = {} & (W_i * L_{d,n}) \cdot C_{jd,n} + (W_i + 2L_{d,n}) \cdot C_{j-sw,n} \\ & + (W_l * L_{d,p}) \cdot C_{jd,p} + (W_l + 2L_{d,p}) \cdot C_{j-sw,p} \end{aligned} \quad (18)$$

5. ASSUMPTIONS FOR ANALYTICAL FORMULATION

In order to simplify the overall expression of the

product $Ad*UGB$, we make the following assumptions:

i) Typically drain extends 4λ beyond the gate, therefore

$$L_{d,n} = L_{d,p} = 4\lambda \quad \ldots (19)$$

where λ is minimum possible dimension in a technology with 2λ as the minimum feature size.

ii) Since the differential gain and unity-gain bandwidth are independent of width of the load transistor, W_l, it can be chosen to be minimum *i.e.* 2λ. Substituting this

$$C_{dbi} = (W_i * 4\lambda) \cdot C_{jd,n} + (W_i + 2*4\lambda) \cdot C_{j-sw,n} \quad (20)$$

$$C_{dbl} = (2\lambda * 4\lambda) \cdot C_{jd,p} + (2\lambda + 2*4\lambda) \cdot C_{j-sw,p} \quad (21)$$

iii) Further, if we approximate that $C_{jd,n} \sim C_{jd,p}$ and $C_{jd,n} \sim C_{jd,p}$, the total load capacitance is given by

$$C_L = C_{dbi} + C_{dbl} = (W_i + 2\lambda) \cdot 4\lambda \cdot C_{jd} + (W_i + 18\lambda) \cdot C_{j-sw} \quad \ldots (22)$$

iv) For most analog applications, to increase the input transistor transconductance, $W_i >> 2\lambda$, which further reduces equation (6.28) to the approximation

$$C_L \approx W_i \cdot 4\lambda \cdot C_{jd} + (W_i + 18\lambda) \cdot C_{j-sw} \quad \ldots (23)$$

Equation (22) can also be written as

$$C_L = W_i \left[4\lambda \cdot C_{jd} + \left(1 + \frac{18\lambda}{W_i} \right) \cdot C_{j-sw} \right] \cdot \ldots (24)$$

Substituting this as the load in equation (6.13) the upper bound on the product $Ad*UGB$ becomes

$$Ad*UGB < \frac{10k_n}{\pi \cdot \left[4\lambda \cdot C_{jd} + \left(1 + \frac{18\lambda}{W_i} \right) \cdot C_{j-sw} \right]} \cdot \left(1 + \frac{L_i}{2.L_l} \right)^{-1} \ldots (25)$$

v) Further, for most analog applications $W_i >> 18\lambda$, then the above eqn. (6.31) further reduces to

$$Ad*UGB < \frac{10k_n}{\pi \cdot \left[4\lambda \cdot C_{jd} + C_{j-sw} \right]} \cdot \left(1 + \frac{L_i}{2.L_l} \right)^{-1} \quad (26)$$

vi) Also, typically $L_i << L_l$, which further reduces the above expression (26) to

$$Ad*UGB < \frac{10k_n}{\pi \cdot \left[4\lambda \cdot C_{jd} + C_{j-sw} \right]} \quad \ldots (27)$$

This is a pure technology constant. Therefore, we can say that the product $Ad*UGB$ is a technology constant.

Even if $L_i << L_l$ is not true, and $L_i = L_l$ as in our case, the equation (26) reduces to

$$Ad*UGB < \frac{20k_n}{3\pi \cdot \left[4\lambda \cdot C_{jd} + C_{j-sw} \right]} \quad \ldots (28)$$

which is also a technology constant.

Equation (25) with $L_i = L_l$, is plotted as a function of W_i for several technologies as shown in Figure 2. Clearly $Ad*UGB$ becomes independent of W_i for wide transistors and is a constant for a technology. It implies that gain of the circuit in a technology can only be increased at the cost of unity-gain bandwidth or vice-a-versa. The value of $Ad*UGB$ at $W_i = 500\mu m$ in various technologies has been plotted in Figure 3. It is evident that in most cases the value of $Ad*UGB$ increases with the scaling of technology.

These results were obtained with no external load connected to the output of the differential amplifier. Only the parasitic drain capacitance loads of the input and load transistors were considered.

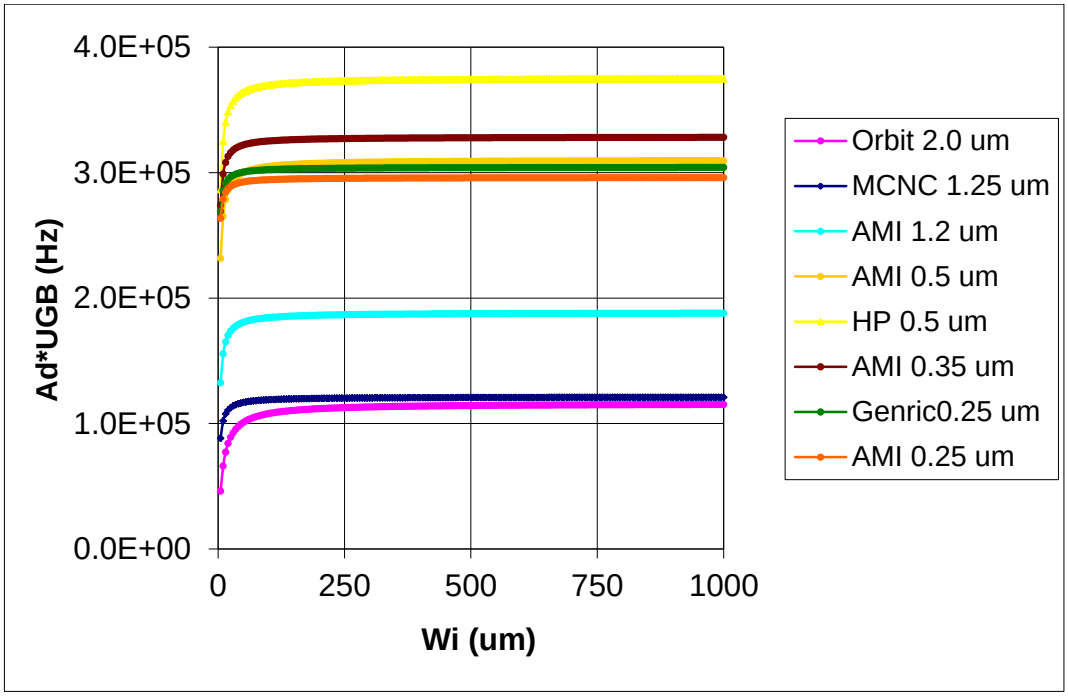

Fig. 2: *Analytical Ad*UGB Product Variation with Technology.*

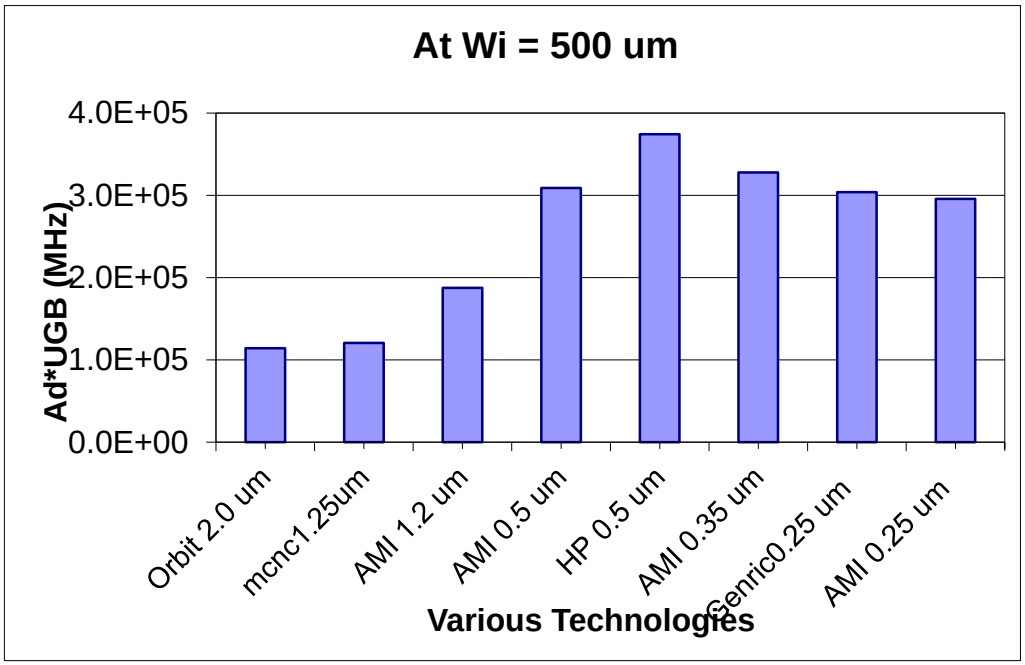

Fig. 3: *Ad*UGB Product Variation at* $W_i = 500\mu m$ *for various Technologies.*

6. DAMPING FACTOR FOR A LOADED DIFFERENTIAL AMPLIFIER

However, given that the unity gain bandwidth, UGB is inversely proportional to the load connected at the output of the differential amplifier, the limiting value of the gain unity-gain bandwidth product, $Ad*UGB$ for an amplifier loaded with external capacitor of value $C_{L(ext)}$ can be worked out as

$$(Ad*UGB)_{loaded} = \frac{(Ad*UGB)*(C_{di}+C_{dl})}{(C_{di}+C_{dl}+C_{L(ext)})} \quad \ldots (29)$$

$$= \frac{(Ad*UGB)}{1+\left(\frac{C_{L(ext)}}{C_{di}+C_{dl}}\right)} \quad \ldots (30)$$

$$= f_{load}*(Ad*UGB) \quad \ldots (31)$$

where f_{load} is a load dependent degradation factor defined by

$$f_{load} = \frac{1}{1+\frac{C_{L(ext)}}{(C_{di}+C_{dl})}} \quad \ldots (32)$$

Equations (30) and (31) provides a rapid way of computing the loaded gain unity-gain bandwidth product, $Ad*UGB$ for any differential amplifier given its unloaded $Ad*UGB$ product. Figure 4 shows how the $Ad*UGB$ product varies with the external load $C_{L(ext)}$.

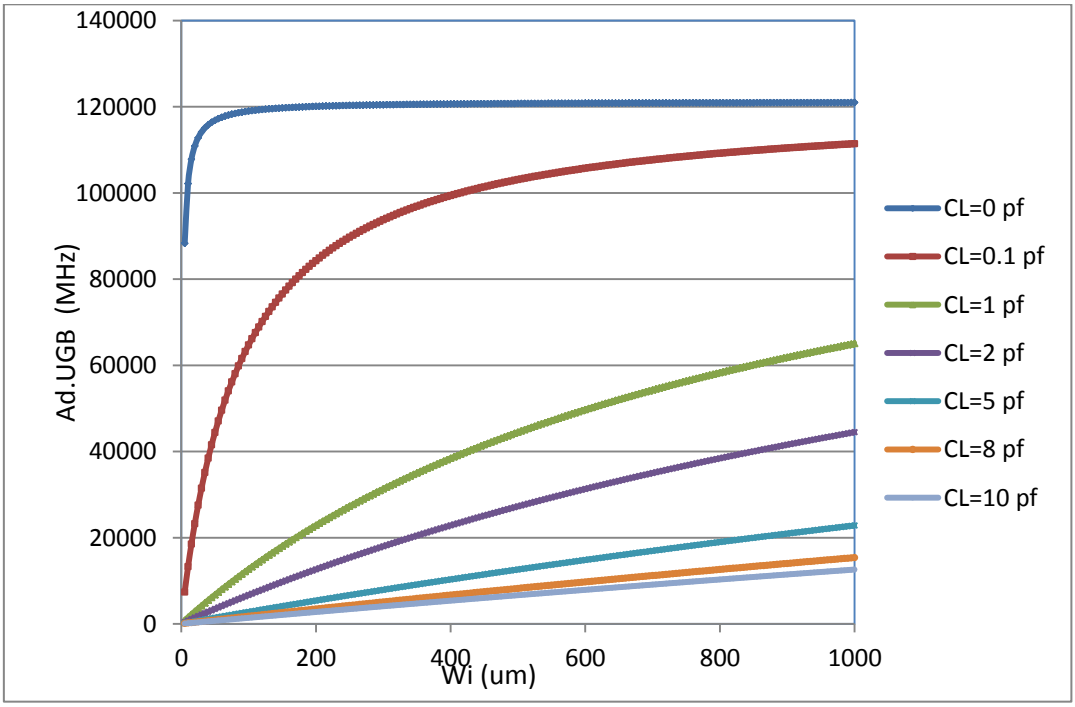

***Fig.4**. Analytical Ad*UGB Product Variation with External Load C_L for MCNC 1.25 µm CMOS Technology.*

7. CONCLUSION

There exits an upper limit for the product ($Ad*UGB$) of differential dc voltage gain (Ad) and unity-gain bandwidth (UGB) of an externally unloaded differential amplifier and this maximum limit is constrained by the technology parameters and hence is a technology constant. Further, as the external load increases, the upper limit of obtainable $Ad*UGB$ product reduces by a degradation factor.

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