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Performance Analysis of $Fe/SiO_2/Fe$ MTJ and $Ni/Al_2O_3/Ni$ MTJ-based Magnetoresistive Random Access Memories (MRAMs)

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ABSTRACT

This paper reports the first principle simulations of $Fe/SiO_2/Fe$ and $Ni/Al_2O_3/Ni$ magnetic tunnel junctions (MTJs). A performance analysis has been done based upon the device-level simulations of the two magnetic tunnel junctions followed by the circuit level simulations of magnetoresistive random access memory (MRAM) cell operating with the two MTJs respectively. From the device-level simulations, the two MTJs have been compared with regard to the bias dependence of TMR ratios, insulator thickness dependence of TMR ratios and insulator thickness dependence of parallel and anti-parallel state resistances taking the relative magnetizations of the two ferromagnetic films of the MTJs into consideration. From the circuit-level simulations, the static and switching power dissipations have been computed along with the delay time estimation.

Keywords: *First principle, magnetic tunnel junction, DFT, ATK, MRAM, TMR, LSDA*

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1. INTRODUCTION

An MTJ is a stack of three layers, one layer on top of the other. The layers at the top and the bottom of the stack are essentially made up of ferromagnetic materials like Fe, Co, Ni, or even the Heusler alloys [1] and there is an insulating layer sandwiched in between the two ferromagnetic layers. These ferromagnetic layers are essentially thin films with a thickness of around 10 nm. The insulator can be MgO, Al_2O_3, SiO_2 or even the high κ materials like HfO_2, ZrO_2 and so on [2]. The thickness of the insulating layer is around 2 nm. These thin films have been deposited using a number of thin film deposition techniques like physical vapor deposition (PVD) which can include sputtering, molecular beam epitaxy, pulsed laser deposition and cathodic arc deposition, and chemical vapor deposition (CVD) and atomic layer deposition (ALD). As the layers at the top and bottom of the stack are ferromagnetic, they possess their own magnetizations respectively. There can be situations when the relative magnetization of the top ferromagnetic layer has parallel or anti-parallel alignment with respect to the alignment of magnetization of the ferromagnetic layer at the bottom of the stack. As the insulating layer is very thin, depending upon the relative orientation of magnetization of the two ferromagnetic layers, electrons from one ferromagnetic layer can tunnel through to reach the other metal layer when a bias voltage is applied across the MTJ. This phenomenon is called spin dependent tunneling (SDT). SDT is an inherent property of MTJs. These MTJs can be used to store data in the magnetization of the ferromagnetic layers and can be effectively used as non-volatile memories. When magnetizations of two ferromagnetic layers are

parallel, a low resistance path is said to exist through the MTJ and electrons can tunnel through the insulator from the topmost layer to the ferromagnetic layer at the bottom. This state corresponds to writing a bit 0. But when the magnetizations of the two layers are anti-parallel, a high resistance path is said to exist through the MTJ and in such cases, most of the voltage drops across the MTJ. This state corresponds to writing a bit 1. In this way, storing a binary bit (either 1 or 0) can be realized using an MTJ [3–5]. But the reason why MTJs did not gain popularity as a non-volatile memory is that there was no way of reading the stored data. This led to the development of MTJ-based magnetoresistive random access memories (MRAMs) which are claimed to be the universal memories. An MTJ-based MRAM cell consists of a transistor with the MTJ on top of it. It accomplishes the write operation using the MTJ and the read operation is accomplished using a field effect transistor (FET). The FET used in MRAMs is an n-channel MOSFET (NMOS) [3]. Accessing the stored data from the MTJ can be done in two ways: direct access and access via the sensing transistor.

Magnetoresistance is the property of a material to change the value of its electrical resistance when an external magnetic field is applied to it. Different magnetic tunnel junctions exhibit different tunnel magnetoresistance (TMR) ratios. TMR is a magnetoresistive effect that occurs in magnetic tunnel junctions (MTJs). Since this process is forbidden in classical physics, TMR is a strictly quantum mechanical phenomenon where the tunneling current depends on the relative orientation of magnetizations of the two ferromagnetic layers, which can be changed by an applied magnetic field or current [6]. The effect was originally discovered in 1975 by M. Jullière (University of Rennes, France) in Fe/Ge-O/Co-junctions at 4.2 K [7]. The read-heads of modern hard disk drives work on the basis of magnetic tunnel junctions. TMR, or more specifically the tunnel magnetoresistance, is the basis of MTJ-based MRAM, a new type of non-volatile memory. In order to quantify the percentage change in the junction resistance, one defines a tunnel magnetoresistance ratio, TMR, in terms of the junction resistances in the parallel and the anti-parallel magnetized states R_P and R_{AP} respectively, where

$$TMR = \frac{\Delta R}{R_{AP}} \times 100\% = \frac{R_{AP} - R_P}{R_{AP}} \times 100\% \quad (1)$$

2. SIMULATION SET UP

In this paper, four different MTJ configurations have been built and they have been simulated for I-V curves for both parallel and anti-parallel magnetization states respectively. The setup used for all the four sets of simulations is shown in Figure 1. The left electrode is grounded while bias voltage is applied to the right electrode. The calculator used here is ATK-DFT (Device). As the I-V curves are a result of spin-polarized electron transport, the exchange correlation used is LSDA (local spin density approximation). The length of each MTJ is around 30 Å and the tunnel barrier is 10.9767 Å thick.

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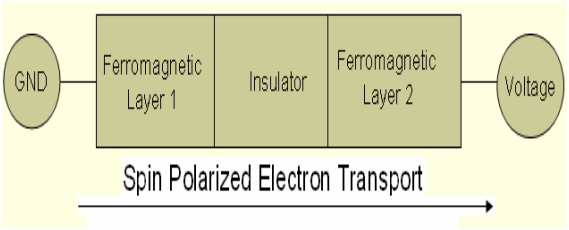
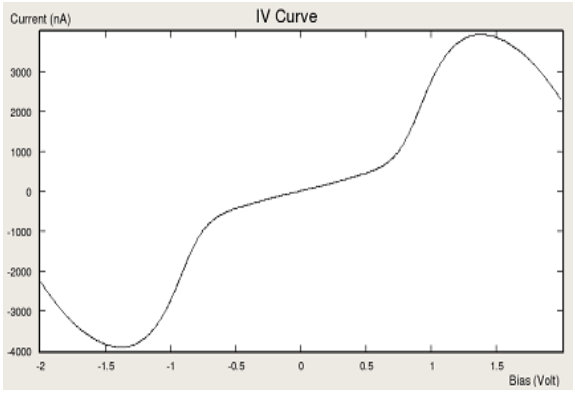


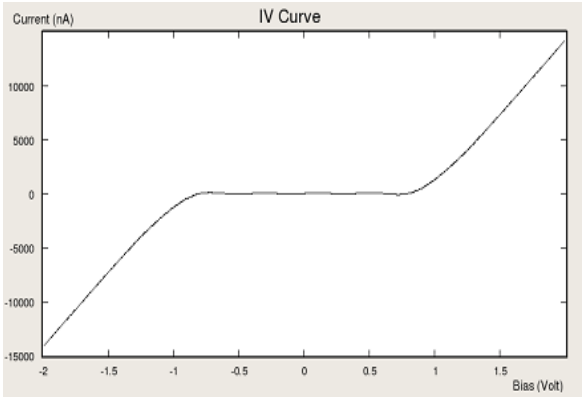
Fig. 1: *Setup Used for Simulation.*

3. SIMULATION RESULTS

Figures 2(a) and (b) depict the I-V curves for parallel and anti-parallel magnetization states of $Fe/SiO_2/Fe$ MTJ respectively. Very high tunnel currents (nearly 3000 nA) can be seen for a bias voltage of 1.4 V and when the bias voltage is further increased, a negative resistance region is observed in the I-V curve for parallel magnetization state. In the anti-parallel magnetization state, for bias voltage up to 1 V, the tunnel current revolves around zero mark and with an increase in bias voltage from 1 V, the tunnel current increases linearly. At 2 V, very high tunnel current of nearly 15000 nA has been reported which is much higher than the magnitude of tunnel currents observed in case of parallel magnetization. This increase in tunnel current can be attributed to the presence of resonant channels in the dielectric in anti-parallel magnetization state. As long as the bias voltage is under 1 V, high resistance state is observed in the anti-parallel magnetization state which is not the case with parallel magnetization state. Figures 3(a) and (b) depict the I-V curves for parallel and anti-parallel magnetization states of $Ni/Al_2O_3/Ni$ MTJ respectively. Ideally, the magnitude of tunnel currents observed in parallel magnetization state should be much greater than that in case of anti-parallel magnetization state. This ideal property is seen in the I-V curves of $Ni/Al_2O_3/Ni$ MTJ in its parallel and anti-parallel magnetization states respectively. A negative resistance region can again be seen in the parallel state I-V curve of $Ni/Al_2O_3/Ni$ MTJ when the bias voltage is increased beyond 0.7 V. Unlike $Fe/SiO_2/Fe$ MTJ, negative resistance regions are evident in the I-V curve of anti-parallel magnetization state of $Ni/Al_2O_3/Ni$ MTJ.

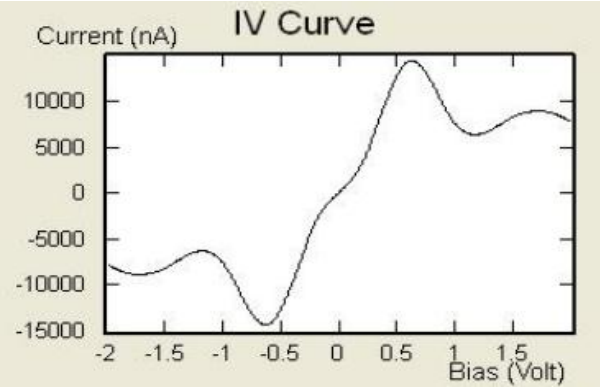


(a)

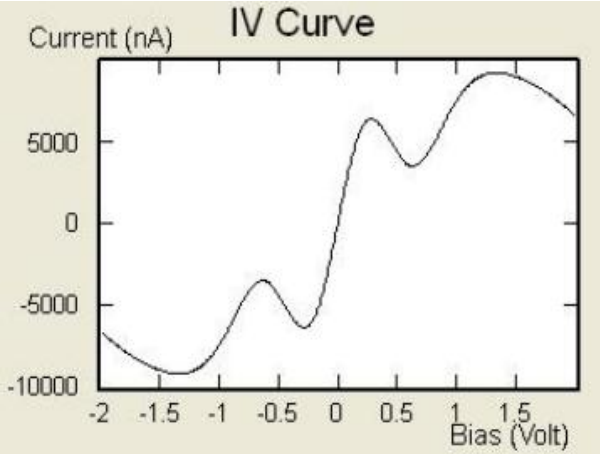


(b)

Fig. 2: I-V *Curves of $Fe/SiO_2/Fe$ MTJ in (a) Parallel and (b) Anti-parallel Magnetization States.*



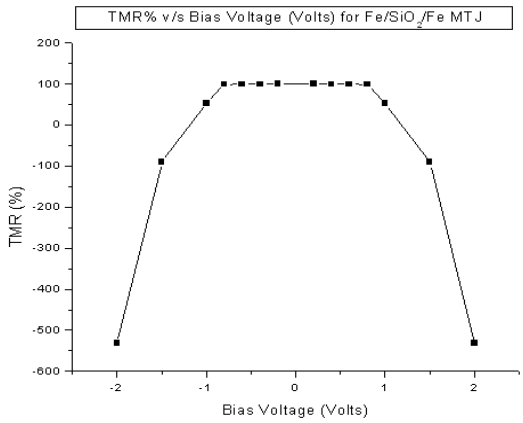
(a)



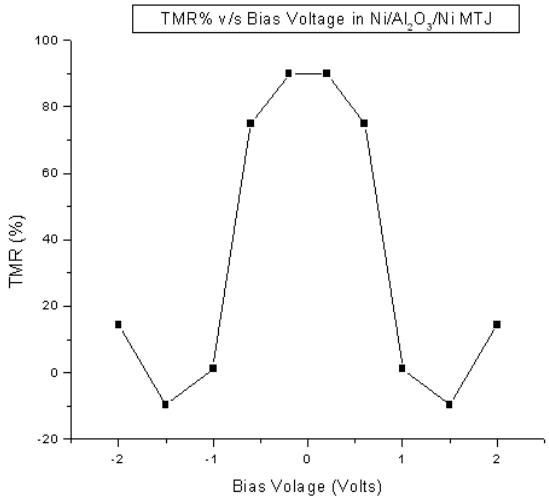
(b)

***Fig. 3: I-V** Curves of $Ni/Al_2O_3/Ni$ MTJ in (a) Parallel and (b) Anti-parallel Magnetization States.*

From these I-V curves, the TMR (%) versus bias voltage plots have been obtained for both the MTJs as shown in Figures 4(a) and (b). The TMR ratios have been calculated using Eqn. (1). For $Fe/SiO_2/Fe$ MTJ, very high TMR ratios have been reported for the bias voltages ranging from −1 V to 1 V. Unlike in $Fe/SiO_2/Fe$ MTJ, near 100% TMR ratio for an extended bias voltage range is not observed in case of $Ni/Al_2O_3/Ni$ MTJ. The maximum TMR ratio obtained in case of $Fe/SiO_2/Fe$ MTJ is 99.8897% for a bias voltage of 0.2 V while the maximum value obtained in case of $Ni/Al_2O_3/Ni$ MTJ is 89.9855% and it occurs at a bias voltage of 0.2 V. The high TMR ratios observed in Fe/SiO2/Fe MTJ can be attributed to the high spin polarization of Fe while in Ni, the spin polarization is comparatively less thereby yielding comparatively lower TMR ratios. An interesting feature observed in the TMR plots of both the MTJs is the negative TMR ratios reported at 1.5 V and 2 V in case of $Fe/SiO_2/Fe$ MTJ and at 1.5 V in case of $Ni/Al_2O_3/Ni$ MTJ. The reason for such an anomalous behavior is not clear and needs to be further investigated in due course of time.



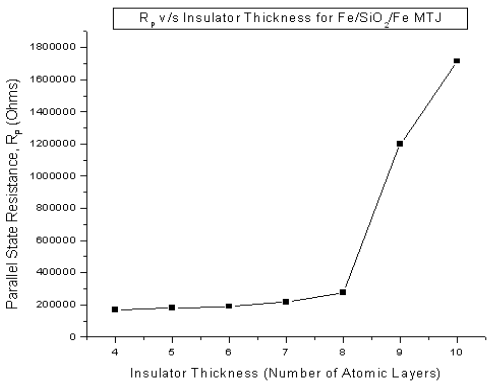
(a)



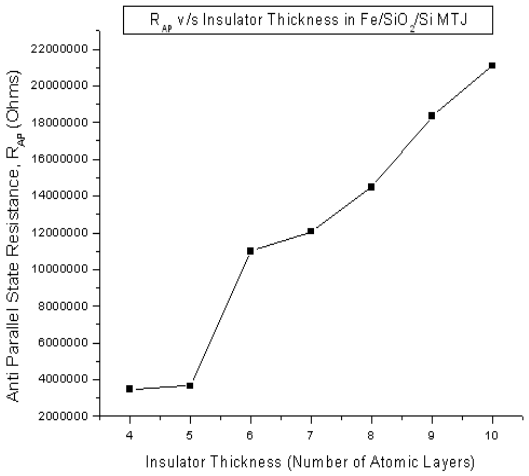
(b)

***Fig. 4:** TMR (%) versus Bias Voltage Plots for $Fe/SiO_2/Fe$ and $Ni/Al_2O_3/Ni$ MTJ.*

In order to study the quality of the insulator used in these MTJs, the thickness of the insulator has been increased from 4 to 10 atomic layers and the corresponding I-V plots have been obtained at 0.5 V for parallel and anti-parallel cases. From these plots, the resistances in parallel and anti-parallel states have been plotted against increasing insulator thickness as shown in Figures 5(a) and (b) for $Fe/SiO_2/Fe$ MTJ and Figures 6(a) and (b) for $Ni/Al_2O_3/Ni$ MTJ respectively. Ideally, with an increase in the insulator thickness, an exponential increase in resistance is expected. The $Fe/SiO_2/Fe$ MTJ meets the expectations and an exponential increase in both parallel and anti-parallel state resistances can be observed, though the magnitude of resistance obtained for anti-parallel state is far greater than those of parallel state as is clear in Figure 5. This ideal behavior is not found in case of $Ni/Al_2O_3/Ni$ MTJ where the resistance in both parallel and anti-parallel magnetization states drops at certain insulator thicknesses as is clear in Figure 6. The sudden drop in resistances can be attributed to the presence of resonant channels within the insulator which increases the conductance through the insulator for certain insulator thicknesses.

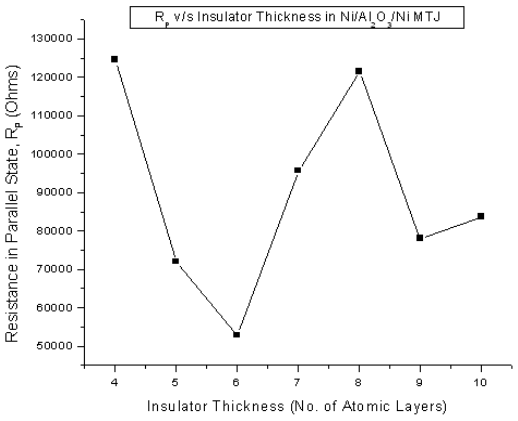


(a)

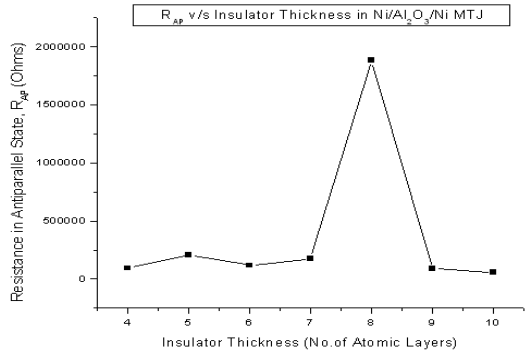


(b)

Fig. 5: *Resistance versus Insulator Thickness Plots for (a) Parallel and (b) Anti-parallel States in $Fe/SiO_2/Fe$ MTJ.*



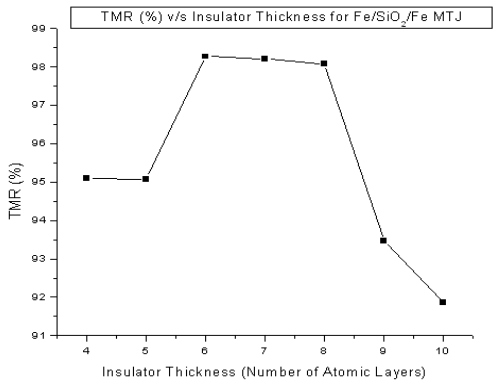
(a)



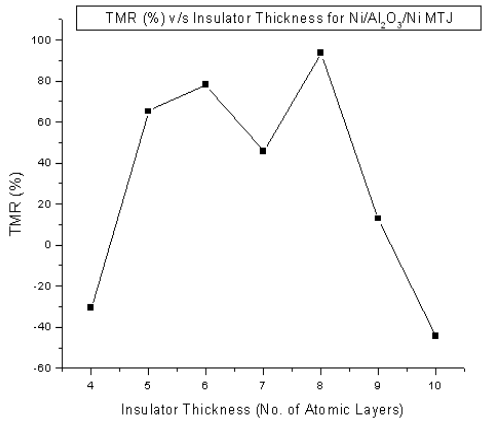
(b)

Fig.6: *Resistance versus Insulator Thickness Plots for (a) Parallel and (b) Anti-parallel States in $Ni/Al_2O_3/Ni$ MTJ.*

Figures 7(a) and (b) depict the plot of TMR (%) with increasing insulator thickness calculated at a bias voltage of 0.5 V for $Fe/SiO_2/Fe$ and $Ni/Al_2O_3/Ni$ MTJs respectively. Zig zag features can be seen in the plots of both the MTJs, though $Ni/Al_2O_3/Ni$ MTJ exhibits negative TMR ratios at insulator thicknesses of 4 and 10 atomic layers.



(a)



(b)

Fig. 7: *TMR (%) versus Insulator Thickness Plots for (a) $Fe/SiO_2/Fe$ and (b) $Ni/Al_2O_3/Ni$ MTJs.*

As the existing circuit-simulating tools do not have a library file that can be used to represent an MTJ in an MRAM circuit, we use a resistor and a capacitor connected in parallel as an equivalent circuit of MTJ. The resistance and capacitance values can be obtained from the device geometry and device level simulations. For a particular bias voltage, we can have two resistance values, R_P and R_{AP}, respectively. But capacitance is independent of voltage and depends only on the device dimensions. Now, the device that has been simulated is very small in size to realize it in practical as it is made up of 48 atoms and the central insulating layer consists of six atomic layers. The cross-sectional area of the simulated MTJs is 0.16 nm^2. As the tool cannot simulate a device comprising as many numbers of atoms as present in a practically realizable MTJ, we calculate the resistances, both R_P and R_{AP}, for the 0.16 nm^2 cross-section structure at a voltage of 1 V. As resistance is inversely proportional to cross-sectional area, we divide the calculated resistance values by a certain factor (factor by which cross sectional area increases) so that we get resistance values corresponding to the device with 525.6932 nm^2 cross-sectional area. The resistance and capacitance values corresponding to the two MTJs obtained for 1 V are shown in Table I. The difference between R_P and R_{AP} is higher in case of $Fe/SiO_2/Fe$ MTJ when compared to $Ni/Al_2O_3/Ni$ MTJ which gives the former an upper hand in terms of determining the HIGH and LOW states of the MTJ output precisely and hence we get two distinct voltage values at the output of the MTJ whereas in case of $Ni/Al_2O_3/Ni$ MTJ, the difference in resistances is small and hence the output of the MTJ may not reveal HIGH and LOW states distinctively. The static power dissipation in the MTJ and corresponding write energy per bit (time = 20 ns, V = 1 V) are calculated and

tabulated in Table II. Using these R and C values, we performed the circuit level simulations of an MTJ-based MRAM cell using mentor graphics design architect. The schematic of the circuit is shown in the form of a block diagram in Figure 8. The circuit is operated at 1 V. The comparator compares the output of the MTJ with the reference voltage and provides a LOW or HIGH output. The C_{MTJ}, though very small, cannot be ignored, as it plays a vital role in determining the output signal. From the circuit simulations, the delay, rise time and fall time have been obtained separately at the outputs of each of these four MTJs. From these data, the switching power dissipation (power dissipated in charging the MTJ capacitor) and work done in charging the MTJ capacitor are computed and presented in Table III, as obtained, using the fall times of MTJ output with R_P and R_{AP}, respectively.

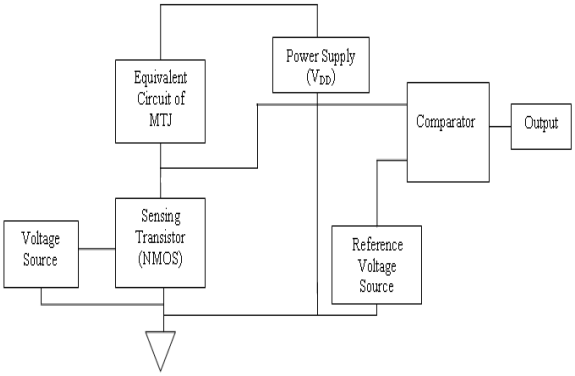


Fig. 8: *Schematic of MTJ-Based MRAM.*

Table I: *Resistance & Capacitance Values.*

MTJ	R_P (Ω)	R_{AP} (Ω)	C_{MTJ} (F)
$Fe/SiO_2/Fe$	110.4838	235.1982	0.0165×10^{-15}
$Ni/Al_2O_3/Ni$	39.2363	58.9635	0.066×10^{-15}

Table II: *Static Power Dissipation and Write Energy per Bit in Parallel and Anti Parallel States.*

MTJ	P_P (W)	P_{AP} (W)	W_P (J)	W_{AP} (J)
$Fe/SiO_2/Fe$	9.05×10^{-3}	4.3×10^{-3}	1.8×10^{-10}	8.5×10^{-11}
$Ni/Al_2O_3/Ni$	0.026	0.0169	5.1×10^{-10}	3.4×10^{-10}

P_P: Power Dissipated in Parallel State, P_{AP} : Power Dissipated in Anti-parallel State, W_P : Write Energy per Bit in Parallel State, W_{AP} : Write Energy per Bit in Anti-parallel State.

Table III: *Switching Power Dissipation and Work Done in charging MTJ Capacitor.*

MTJ	P_P(J/s)	P_{AP}(J/s)	W_P(J)	W_{AP}(J)
$Fe/SiO_2/Fe$	2.9×10^{-12}	1.3×10^{-11}	3.2×10^{-22}	4.1×10^{-21}
$Ni/Al_2O_3/Ni$	3.3×10^{-12}	1.5×10^{-12}	4.6×10^{-22}	3.3×10^{-12}

It can be seen from Table II that $Fe/SiO_2/Fe$ MTJ outscores $Ni/Al_2O_3/Ni$ MTJ in terms of the power dissipated in parallel state, power dissipated in anti-parallel state, write energy per bit in parallel and anti-parallel states.

In terms of switching power dissipation and work done in charging the MTJ capacitor, Fe/SiO_2/Fe MTJ exhibits a lesser magnitude of switching power and requires minimal work done to charge the MTJ capacitor when compared to that of Ni/Al_2O_3/Ni MTJ as is clear from Table III. Also, the Fe/SiO_2/Fe MTJ exhibits impressive rise delay, fall delay, rise and fall times as seen from the data in Table IV.

Table IV: *Rise Delay, Fall Delay, Rise and Fall Time Estimations in Parallel and Anti Parallel States.*

MTJ	Rise Delay with R_P (ps)	Rise Delay with R_{AP} (ps)	Fall Delay with R_P (ps)	Fall Delay with R_{AP} (ps)	Rise Time with R_P (ps)	Rise Time with R_{AP} (ps)	Fall Time with R_P (ps)	Fall Time with R_{AP} (ps)
Fe/SiO_2/Fe	314.9	314.9	330.3	331.6	340.7	400.5	317.9	318.2
Ni/Al_2O_3/Ni	314.8	314.8	330.5	331.3	340.7	401.8	317.8	317.8

4. CONCLUSIONS

In this paper, the LSDA band structure calculations have been carried out for two different magnetic tunnel junctions– Fe/SiO_2/Fe and Ni/Al_2O_3/Ni to obtain the I-V curves in parallel and anti-parallel magnetization states for each of the tunnel junctions. From the I-V curves of each MTJ, the TMR ratios have been computed and plotted against the bias voltages. Fe/SiO_2/Fe MTJ exhibits very high TMR ratios for a wide range of bias voltage when compared to the other simulated MTJ. Also, for a fixed bias voltage of 0.5 V, both the MTJs have been simulated for increasing insulator thicknesses to obtain I-V curves for both parallel and anti-parallel magnetization states. An exponential increase in parallel as well as anti-parallel magnetization state resistance with increase in insulator thickness is observed in Fe/SiO_2/Fe MTJ while the increase is neither very high nor stable in case of the other MTJ. A plot of TMR ratio versus insulator thickness has been plotted for both the MTJs. A block diagram of the schematic of MTJ-based MRAM cell circuit has been proposed and the schematic has been simulated for both the MTJs by extracting the resistance and capacitance values from the device level calculations. From the circuit-level simulations, the static power dissipation and write energy per bit have been found to be the least in case of Fe/SiO_2/Fe MTJ which also exhibits impressive rise delay, fall delay, rise time and fall time. The switching power dissipation and work done in charging the MTJ capacitor in both parallel and anti-parallel magnetization states suggests that Fe/SiO_2/Fe dissipates a relatively lower switching power when compared to the other MTJ thereby proving Fe/SiO_2/Fe MTJs to be faster than the others. Therefore, it can be concluded that Fe/SiO_2/Fe MTJ is the better suited MTJ for MRAMs

owing to its very high TMR ratios for a wider voltage range, good quality of insulator as seen from the exponential increase in parallel and anti-parallel resistances with increasing insulator thickness, least static power dissipation and write energy per bit and impressive switching power dissipation, work done in charging the capacitor, rise delay, fall delay, rise time and fall time. Therefore, MTJ-based MRAMs are a strong contender to replace the age old flash memories in cell phone architectures and other low power, high speed applications since they can be scaled down to a much greater extent to attain a feature size that is much smaller than DRAMs and other existing memory technologies. MTJ-based MRAMs do not need to be periodically refreshed like DRAMs, they are non-volatile, very small in size, much faster than modern day memories, consume much less power and operate faster than other memory technologies.

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