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Low Power High Speed Eight-Transistor (8T) SRAM Cell with Enhanced Data Stability

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Abstract

The demand of static random access memory cell in embedded memories is rapidly increasing. To design SRAM is continuously becoming difficult due to limitation of weaker write margin, degraded data stability and higher leakage power consumption. In order to overcome these limitations, new 8T SRAM has been explored. The simulation results depicts better data stability, low access delay and decreased leakage power consumption. Alternatively, proposed cell with sleep transistor and cell with dual threshold voltage (DVT) is designed, also. The evaluated parameters of all the circuits are compared with conventional 6T SRAM cell. When comparison of the different parameters carried out, the new 8T SRAM cell shows the data stability is increased up to 47.5% and 33.7% during read operation and hold state respectively as compare to conventional 6T SRAM cell. The results depict, read and write access delay is deducted up to 27.9x and 55.6x respectively when compared with 6T SRAM cell. Additionally, the new 8T SRAM circuit with DVT consumes 2.842pA leakage current, which is 92.05% less than 6T SRAM cell.

Keywords: *SRAM, DVT, data stability, write margin*

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INTRODUCTION

In Modern integrated circuits demand continuous down scaling of process technology which leads to higher integral density and challenges to optimize the performance of the circuit in terms of leakage current, access delay and stability [1]. Today's era of technology highly demands static random access memory as a main part of ICs design. That is facing severe problems like power dissipation, leakage current and stability [2, 3]. Supply voltage minimization can reduce total power dissipation but it affects adversely on read static noise margin and hold static noise margin of the cell. Hence, degrades data stability during read and hold operation of the cell [4]. This constraint effects the normal operation of conventional 6T SRAM cell at ultralow power supply. Conventional 6T SRAM cell has a limitation of read disturbance during read operation [5] that results in poor read static noise margin. The read static noise margin can be improved by totally disconnecting the bit lines from the storing nodes. This can be achieved by using differential word-lines for write and read operations [6].

Figure 1 presents the conventional 6T SRAM cell. As, it scaled down, data stability of the cell is not reliable. This is due to low signal levels at low supply voltages. Additionally, at low supply voltages due to flipping of stored content at the storing nodes Q and QBAR, it is not easy to analyze the performance of the cell [6, 7]. Which results in intrinsic read disturbance produces in conventional 6T SRAM cell. Hence, it affects the data stability and functionality of the circuit in SRAM designing. Another idea to maintain the performance of the cell is to look over the beta ratio (β) where β is defined as the size of pull down NMOS transistor to the size of NMOS access transistor [7]. To enhance the performance of the 6T SRAM cell in terms of the write and read margin various methods have been presented such as, power gating and ground gating techniques.

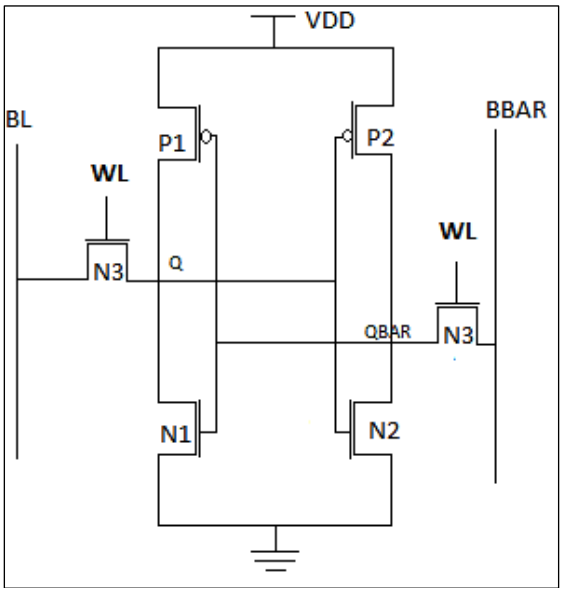

Fig. 1: *Conventional 6T SRAM Circuit.*

Alternatively, contribution of leakage current is high in total power dissipation. It flows through the circuits, when the circuit is in standby mode [8]. By utilizing high threshold voltage transistors in the circuit leakage current can be minimize to some extend [7–9].

A new 8T SRAM cell is presented for providing lower leakage current and high data stability. Due to single bit-line, the new 8T SRAM circuit reduces the active power consumption and leakage current [10]. The new 8T SRAM cell utilizes an extra transistor WL, which cut-off the feedback between cross-coupled inverters increases the data stability. The circuit with sleep transistor and putting the cross-coupled inverters (of the cell) on high threshold voltage is also explored. The effect of these techniques on the new 8T SRAM cell is examined. The sleep transistor helps to reduce the leakage current [11] whereas, circuit with DVT provides improved data stability and further reduces the leakage current during hold state [12].

NEW 8T SRAM CIRCUIT

In this paper, a new 8T SRAM cell utilizes 70 nm technology is proposed to provide high speed and improved data stability. The new 8T SRAM cell is shown in Figure 2. In the circuit, there are two cross coupled inverters composed of P1, P2, N1 and N2. Data is stored on the storing nodes Q and QBAR. The circuit consists of only one bit-line BL and differential word-lines WWL and RWL. WWL for write operation and RWL is for read operation. WWL has been enabled during write operation while for read operation RWL is activated. An extra transistor WL (N5) is inserted between two inverters to control active and sleep state of the cell. WL cuts off the feedback between two inverters that, restricts flipping of cell content stored at the nodes Q and QBAR. In left inverter composed of P1 and N1, an extra transistor P3 is inserted, which is connected to WWL. Table 1 shows the truth table of new 8T SRAM for different modes of operations.

Table 1: *Truth Table for New 8T SRAM Cell.*

Different Modes of Operation	RWL	WWL	WL	BL
Read	1	0	1	1
Write	0	1	0	1/0
Hold	0	0	1	1/0

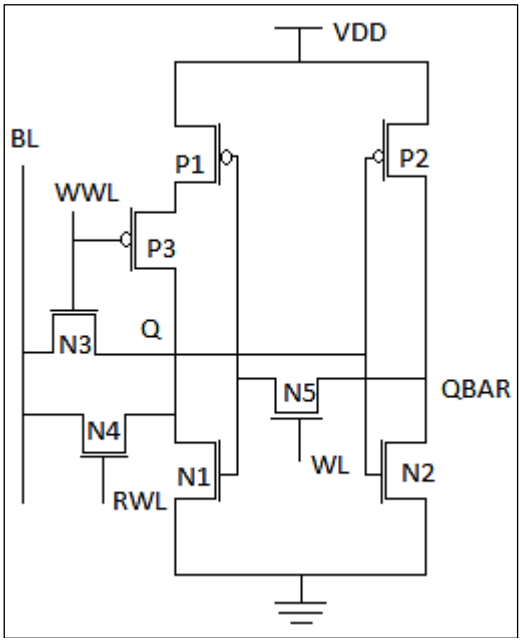

Fig. 2: *New 8T SRAM Circuit.*

WRITE OPERATION

To perform the write operation BL is set to V_{DD} or to 0v, according to the values we want to write on the storing node Q. Hence the cell is single ended; WWL is set to V_{DD} while RWL is maintained at 0v. During write operation, due to turn off state of WL, stored data do not flip, in this condition cell is able to write data perfectly at the storing nodes. While performing write 1, due to having turn off state

of P3, transistor N3 is not able to transmit the full supply voltage at the storing node Q. The voltage at the storing node Q is 1v in the new 8T SRAM cell when the supply voltage used is 1.2, during write 1 operation. So the written bit is 200 mV less than the V_{DD}. During write 0 operation, the cell is able to write perfect 0 at node Q and complementary value at QBAR. So while performing write operation, disable state of WL helps to cut off the feedback between two inverters. After write operation WWL transitions low, in this state the cell switch to the idle state. And the signal WL switches to V_{DD} **w**hereas RWL remain in low state.

READ OPERATION

The before initiating is single ended read operation RWL and WWL transitions high and low respectively. BL and WL charged to VDD. As a result of enabling read word-line N4 transitions in ON state. When 1 is stored at Q, complementary value 0 is stored at QBAR which makes the transistor N1 in off state. Due to off state of N1, BL charged remain as it is, and directly read by the sense amplifier. However, during read 0 operations N4 and N1 both become in turn on state, hence the charged BL gets discharged through N4 and N1. Thereby 0 is read by sense amplifier. In new 8T SRAM cell during read operation the stored data do not float. Hence, reduces the risk of leakage current. Because floating data leads to leakage current during read operation also.

CHARACTERIZATION OF NEW 8T SRAM CIRCUIT USING SLEEP TRANSISTOR AND DUAL THRESHOLD VOLTAGE CIRCUITS

This part of the paper depicts the characterization of the new 8T SRAM cell by utilizing sleep transistor and DVT. Where DVT is for dual thresh hold voltage transistor. Dual threshold voltage transistors are utilized in the circuit to make compromise between high threshold transistors (HVT) and low voltage transistors (LVT) where HVT limits the leakage current of the circuit during idle state of the circuit while LVT are used to get high speed devices. Transistor with thin line represents LVT whereas transistor with thick line represents HVT [13].

NEW 8T SRAM CIRCUIT WITH SLEEP TRANSISTOR

Figure 3 shows the proposed cell with sleep transistor. An HVT, NMOS (N6) sleep transistor is connected serially with N1. During the active mode sleep transistor N6 is kept ON. That assists to keep the ground voltage value at 0 volts. In standby mode of the circuit, the sleep transistor has been disabled. At this state the sleep transistor reduces the leakage current [14, 15].

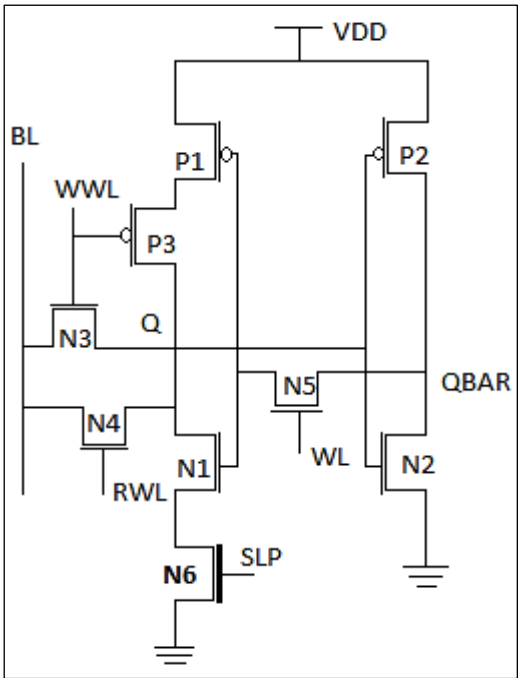

Fig. 3: *Proposed 8T SRAM Circuit with Sleep Transistor.*

NEW 8T SRAM CIRCUIT WITH DVT TECHNIQUE

The new 8T SRAM cell utilizing dual threshold voltage technique is shown in Figure 4. In this particular circuit, the two cross coupled inverters composed of P1, N1 and P2, N2 are kept on high threshold voltage whereas, except those transistors all are kept on low threshold voltage. The main reason to put the inverters on HVT is to lessen the leakage current during hold state and to increase the data stability [7]. Utilizing high threshold voltage (HVT) transistors in SRAM cell increases the cell stability but it inversely effect the write margin whereas the low threshold voltage transistor (LVT) enhances the write ability but decreases cell stability [16, 17].

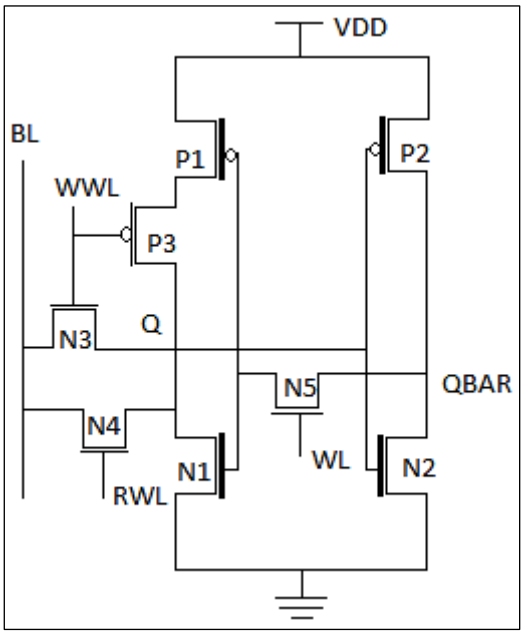

Fig. 4: *New 8T SRAM Circuit with DVT.*

SIMULATION AND RESULTS

In this section, new 8T SRAM cell, new 8T SRAM cell with sleep transistor, new 8T SRAM cell with DVT technique are simulated and analyzed. The comparison has been performed with conventional 6T SRAM cell on the basis of different parameters such as access delay, leakage current and data stability. The circuits are implemented using 70 nm technology node and 1.2 volts supply voltage. Circuits are simulated on the tanner tool. Schematic has been designed on S-Edit and T-spice is used for simulations.

READ AND WRITE DELAY CALCULATIONS

Read delay of SRAM cell is calculated by the maximum time interval from the 50% rise of word line to the 50% fall of sense amplifier output. New 8T SRAM cell utilizes separate read word (RWL). The read access delay of 8T SRAM cell is the longest time interval from the 50% rising edge of RWL to the 50% falling edge of sense amplifier output [7]. Write delay of SRAM cell is maximum time interval from the 50% rising edge of word line to the 50% falling edge of storing node (Q or QBAR) [18]. The values of read and write access delay is shown in Table 2 and Figure 4 reflects the graph.

WRITE MARGIN

Write ability of the SRAM cell is estimated by write margin. The largest amount of noise voltage desired to invert the stored content of the cell, defines the write voltage margin [7]. To calculate write margin, bit-line voltage is swept from 0v to V_{DD}. The value of bit-line voltage, where the storage nodes Q and QBAR crosses each other is used to evaluate write margin [19]. Table 2 and Figure 5 shows the write ability of new 8T SRAM cell and conventional 6T SRAM cell.

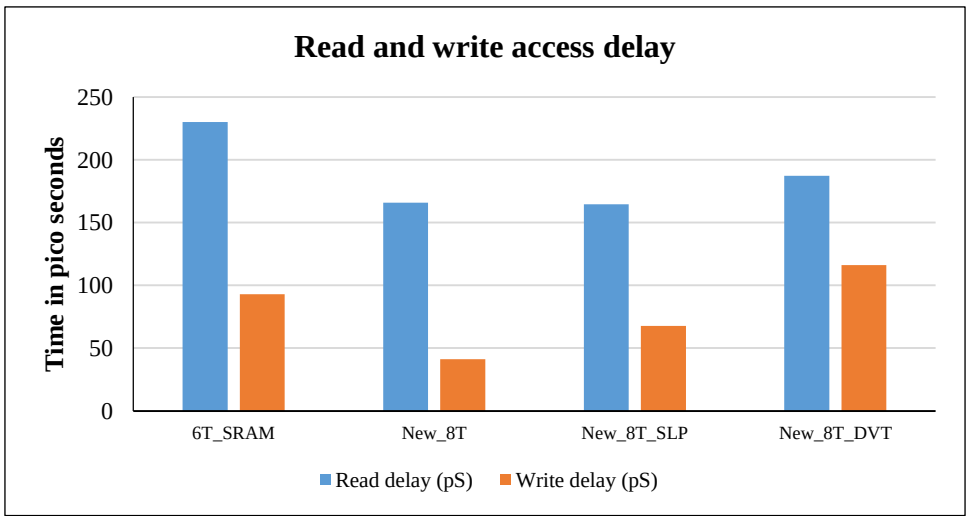

Fig. 5: *Comparison of Write and Read Access Delay.*

READ STABILITY AND HOLD STABILITY

Due to remarkable supply voltage reduction and scaling of transistor size, data stability of SRAM cell is also degrading. It produces a constraint against enhancing performance in terms of stability of the cell at nano meters technology nodes. The term "stability" is reflection of the static noise margin (SNM) of the cell [13]. SNM is the maximum value of noise voltage that a cell can tolerate, and able to restrict the flipping of the saved content. The SNM can be calculated by plotting butterfly curves. It is a graphical method in which voltage transfer characteristic of both the inverters are drawn [20]. The maximum size square lying inside the lobes, gives the value of SNM. Table 2 and Figure 6 shows the graph of stability during read and write state.

LEAKAGE CURRENT AND LEAKAGE POWER CONSUMPTION

In leakage current and leakage power consumption, the leakage current flowing through the cell during the idle state is calculated. Supply voltage scaling reduces active and leakage power consumption but degrades data stability. In this paper to reduce leakage power consumption, sleep transistor and high threshold voltage transistor (HVT) are utilized [21]. Figure 7 shows the graph of leakage current and leakage power consumption [22].

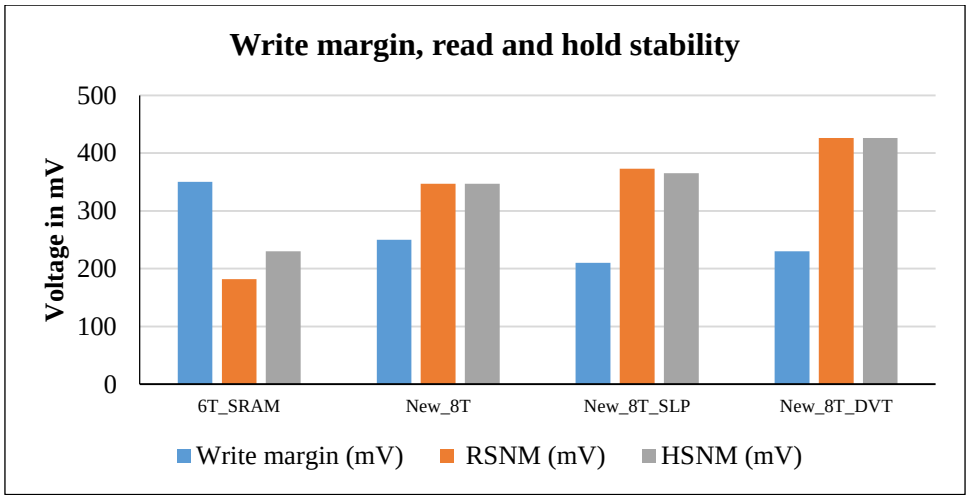

Fig. 6: *Comparison of Write Margin and Data Stability in mV.*

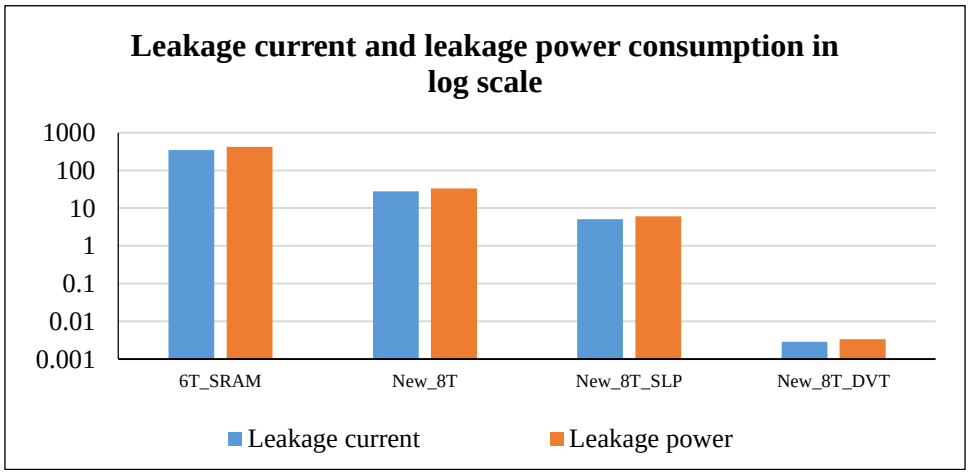

Fig. 7: *Comparison of Leakage Current and Leakage Power Consumption.*

Table 2: *Simulation Results of Different Parameters of 6T SRAM Cell and Proposed 8T SRAM Cell.*

Different parameters	6T SRAM cell	New 8T SRAM cell	New 8T SRAM cell with sleep Transistor	New 8T SRAM cell with DVT
Read delay (pS)	230.10	165.80	164.58	187.31
Write delay (pS)	92.87	41.21	41.07	115.99
Write margin (mV)	350	250	210	230
RSNM (mV)	182	347	373	426
HSNM (mV)	230	347	365	426
Leakage current (in Amp)	349.104 nA	27.74 nA	5.074nA	2.842pA

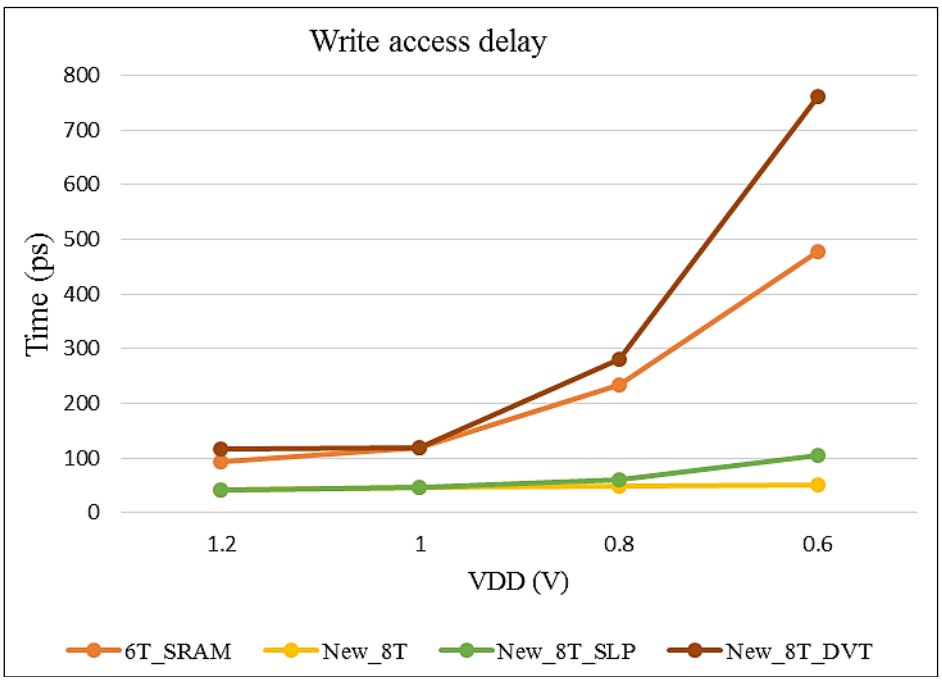

Fig. 8: *Write Delay Comparison at Different VDD.*

IMPACT OF SUPPLY VOLTAGE VARIATIONS

In this section the effect of supply voltage reduction is performed on all the parameters. As discussed previously, the supply voltage degradation minimizes power dissipation, but adversely affects the stability of the cell. Here, the supply voltage range adopted is from 0.6 V–1.2 V. Additionally, width and length of the transistor also affects the performance of the cell. Adjusting the W/L ratio of transistor read margin and write margin can be varied. For, improving the write margin the width of the access transistor should be capable to overcome the pull up transistors. Write margin can be improved by increasing the width of the pull-down transistor. Moreover, using high threshold voltage (HVT) transistors in SRAM

cell increases the cell stability but it inversely effect the write margin. Whereas the low threshold voltage transistor (LVT) enhances the write ability but decreases cell stability. Figures 8 and 9 give the speed performance of the conventional 6T SRAM cell and proposed cell. It can be concluded that with the reduction of supply voltage, read and write access delay of the cell increases. Figures 10 and 11 shows the read stability and write margin respectively. While minimizing the supply voltage, read stability and write margin degraded. Supply voltage scaling has positive impact on leakage current. Figure 12 reflects the impact of voltage degradation on leakage current.

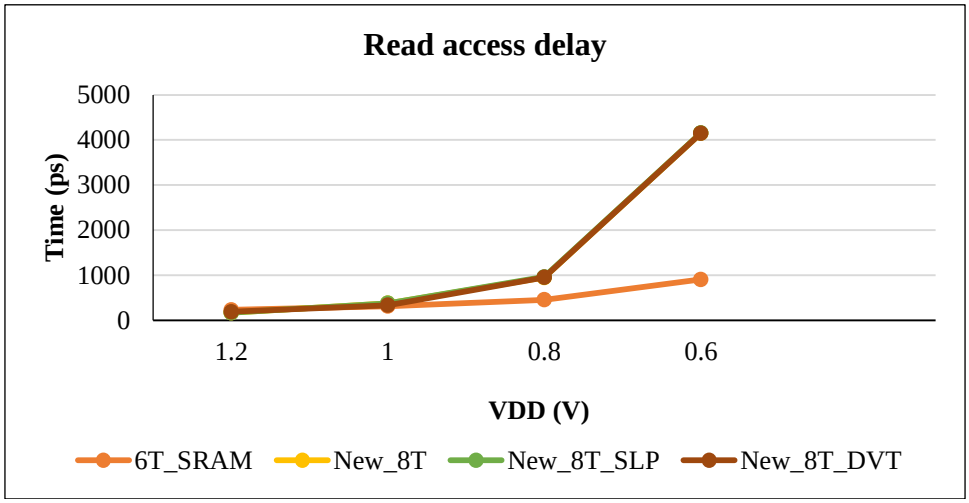

Fig. 9: *Read Delay Comparison at Different VDD.*

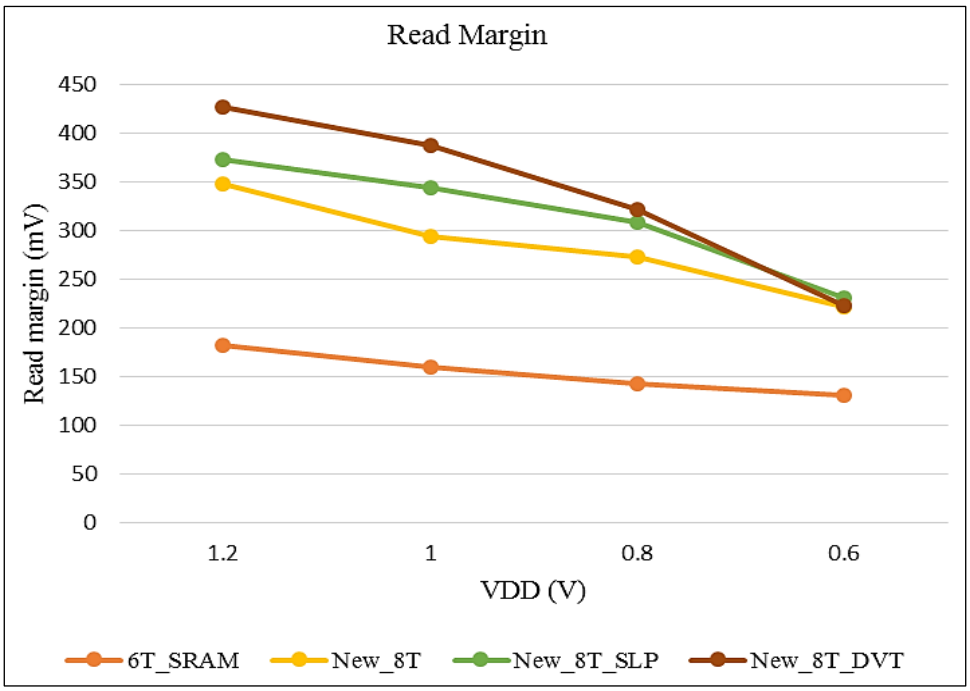

Fig. 10: *Read Stability at Different VDD.*

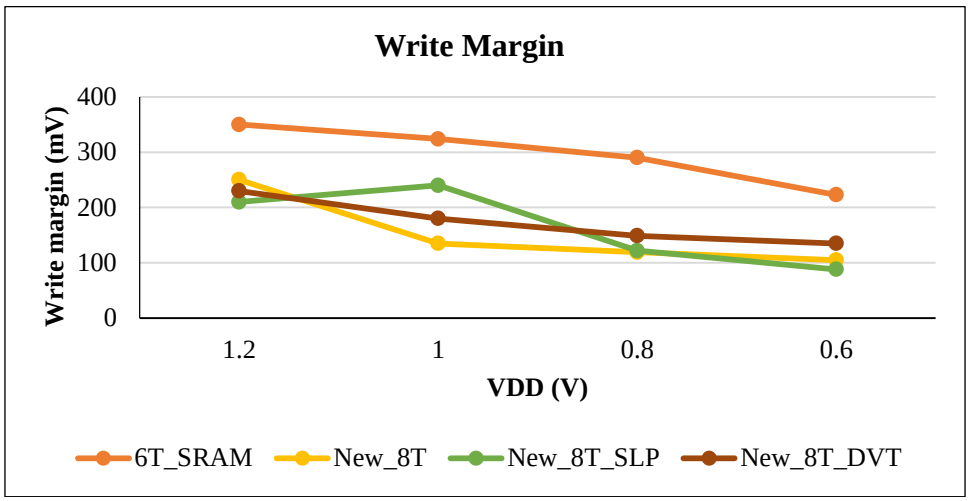

Fig. 11: *Write Margin at Different VDD.*

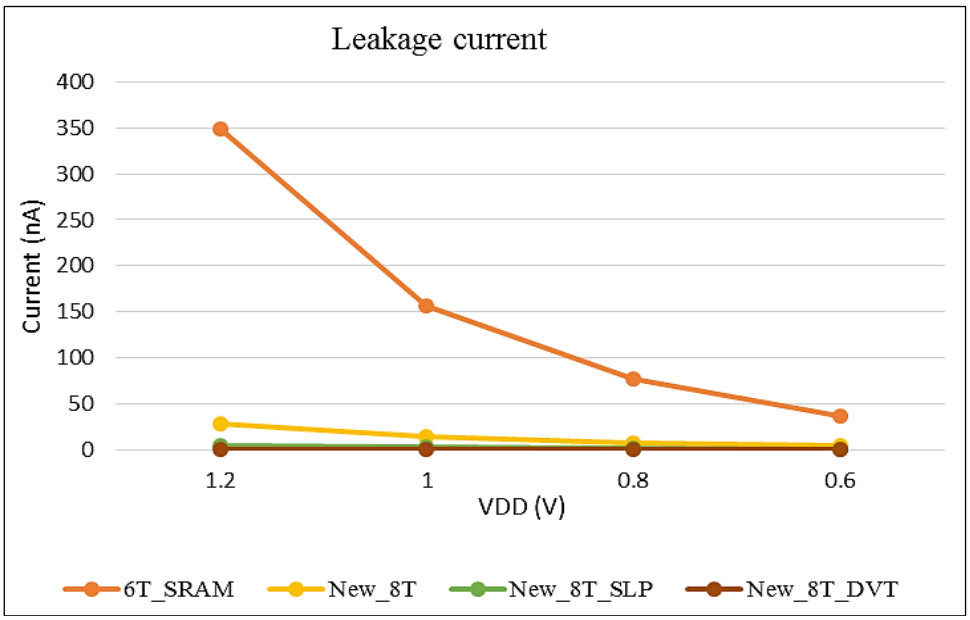

Fig. 12: *Leakage Current at Different VDD.*

CONCLUSION

A new 8T SRAM circuit with low leakage current and high speed performance is explored in this paper. The application of sleep transistor and dual voltage transistor is reviewed here to enhance the performance of the proposed circuit. In this paper the new 8T SRAM cell is analyzed and compared with conventional 6T SRAM cell. The proposed cell increases the data stability up to 47.5x and 33.7x during read operation and hold state respectively as compare to conventional 6T SRAM cell. The results depict, read and write access delay is deducted up to 27.9x and 55.6x respectively when compared with 6T SRAM cell. Additionally, the new 8T SRAM circuit with DVT consumes 2.842 pA leakage current, which is 92.05% less than 6T SRAM cell. By utilizing high threshold voltage (HVT) transistors in SRAM cell, reflects enhance cell stability but degrade the write margin. The proposed cell with DVT further improves the data stability by 22.7x during read and hold state.

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