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Design of CMOS AM Modem for Wireless Sensors

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ABSTRACT

A design of amplitude modulated (AM) modem, compatible to CMOS technology for its monolithic integration with either wireless microsensors or other sources of baseband signals, is presented in this paper operating in different frequency bands. Circuits functional in different operating conditions are considered in the paper to satisfy the requirement from low- to high-speed signals produced either from the wireless sensor or other signal source to be modulated on a MHz or GHz carrier signal in the industrial scientific and medical (ISM) band. Different modem circuit designs are presented in the paper right from the module up to the schematic level after their analysis, circuit simulations are carried out using spice with its equivalent Hspice MOS model level 13 for the CMOS process of SCL 1.2 micrometer semiconductor foundry.

Keywords: *CMOS AM modulator, squarer, rectifier, RF IC, envelop detector*

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1. INTRODUCTION

The paper describes the proposed implementation, in a standard 1.2 μm CMOS technology for a low voltage and low power AM modem circuit that is the core of a transceiver system. It can be used to decode a signal carrying information from an external device to an implantable system.

The carrier frequency is taken as 20 MHz with combination of 18 kHz or lower range frequency signals from the wireless sensors. Further, the design is improved to reduce noise content in the device with various signal frequencies in MHz range and carrier frequencies in GHz range. Comparative studies are carried out for different ranges of the signal with specification of the circuit. A non-standard topology is proposed, allowing the circuit to be fully integrated, thus, lowering the component count of the system and increasing reliability.

2. CIRCUIT DESCRIPTION

Designs presented in this paper have three major components such as AM modulator, squarer and rectifier used as an envelope detector for data extraction. These are illustrated here one by one.

2.1. AM Modulator

This circuit uses two signal generators to produce an amplitude modulated RF carrier at output port V_m. First is the lower frequency signal (V_s) with typical frequency from MHz to kHz or lower frequency range and second is the local oscillator (LO) carrier (V_c) with typical frequency from 200 MHz to GHz RF range. The two signals are mixed and amplified by the MOS transistor as shown in Figure 1 and an amplitude modulated signal appears at the output node V_m (see the response in Figure 2). Input carrier of magnitude 1 V at 10 MHz and audio signal of magnitude 500 mV at 18 kHz, when applied produces the modulated output signal of magnitude ± 8 mV.

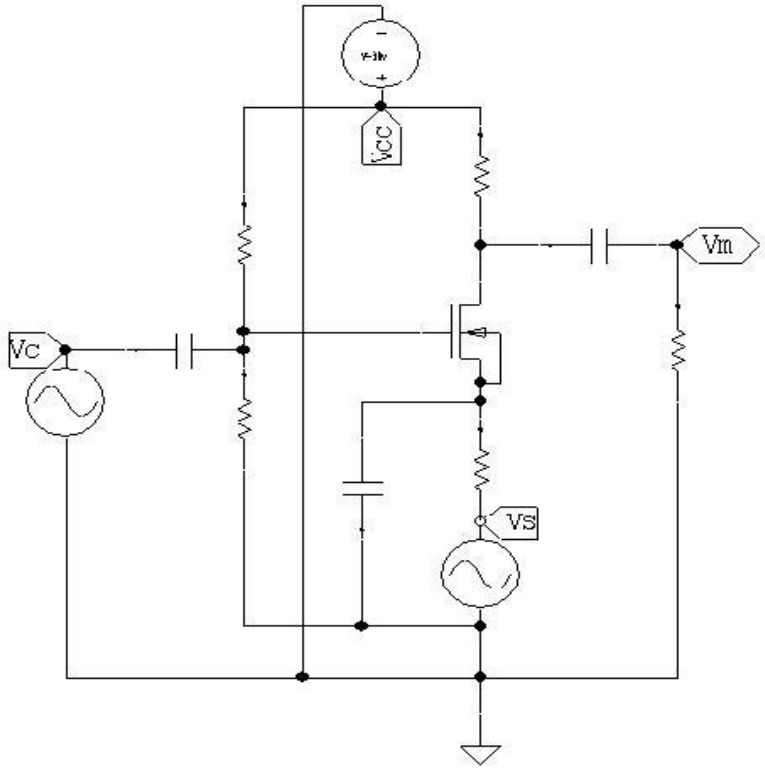

Fig. 1: *AM-Modulator.*

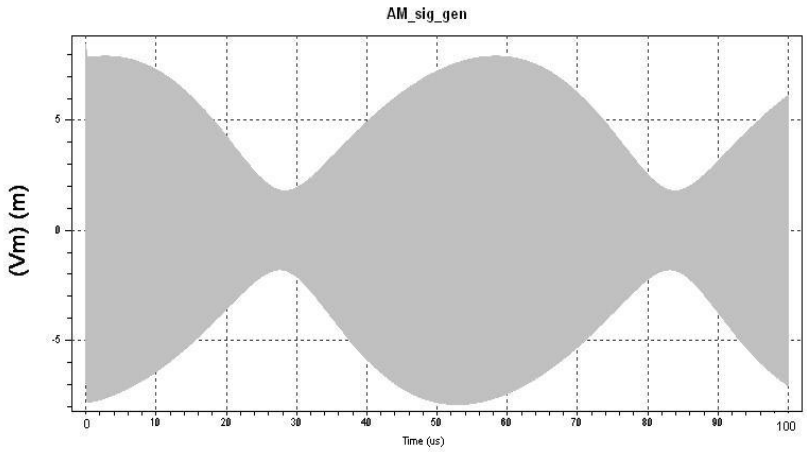

Fig. 2: *Modulated Output.*

2.2. Squarer

In this design, two types of squarers are used. First one uses the squarer as a multiplier [4] where differential outputs are connected to the modulated output (V_o) generated by AM-modulator where V_s and V_c are the same inputs. After analyzing the result, it is replaced by another squarer [1]. Both squarers are shown in Figures 3 and 4.

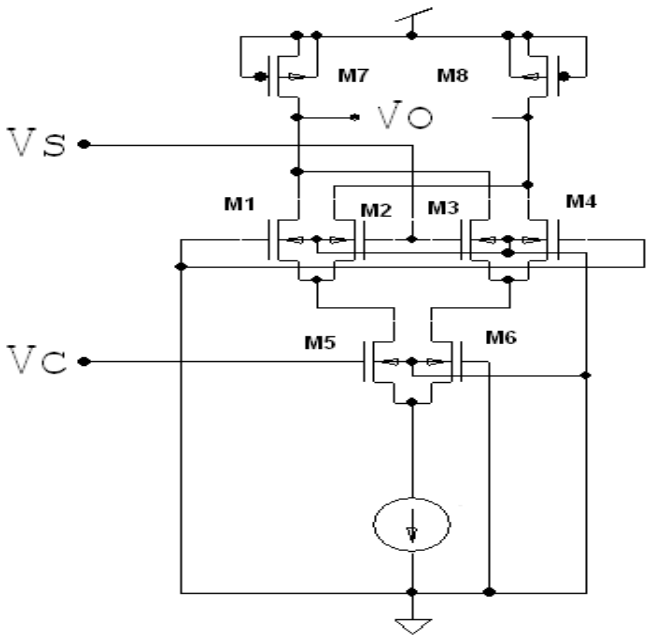

Fig. 3: *Squarer Using Mixer.*

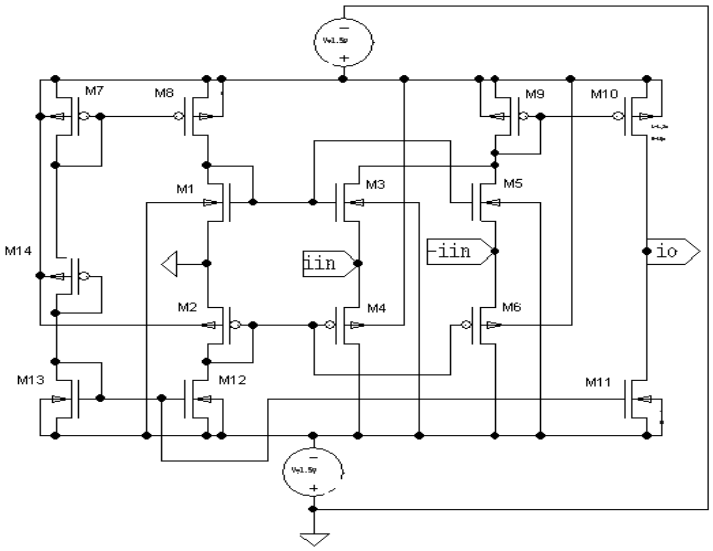

Fig. 4: *A CMOS Current-Mode Squarer/Rectifier Circuit* [1].

2.3. Envelope Detector

There are different ways to demodulate an AM signal and recover the transmitted waveform. Probably the simplest way is to use an envelope detector. Since the modulating signal rides on carrier amplitude and thus forms the envelope in the modulated signal, the envelope detector recovers the modulating signal riding on the carrier by extracting the envelope of the received signal. In Figure 4, a rectifier [1] circuit is used for the same purpose with improved outputs.

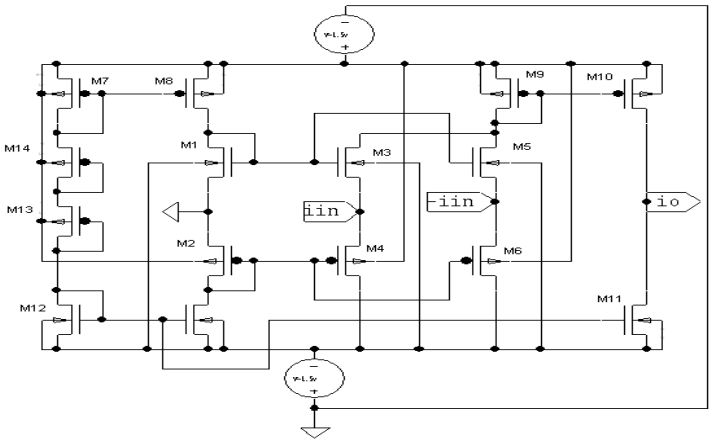

Fig. 5: *Rectifier Circuit Used for Envelop Detection* [1].

3. PRINCIPLE OF OPERATION

Modulated signal is generated through a single transistor in contrast with RC pair for desired output, which serves as the input of the multiplier to reduce the noise contamination at the output. In Figure 3, a single MOSFET operating in the active region [2–5], its first order I-V characteristic behaves according to the square-law relationship.

$$Id = (½\mu_n C_{ox} W/L) * (Vgs - V\ d)^2 \quad (1)$$

For a MOSFET differential pair, the device share the tail current according to the following relation.

$$I_1 + I_2 = I_T \quad (2)$$

Combining equations (1) and (2), drain currents become

$$I_1 = I_T/2 + ½V_d\sqrt{[K(2I_T - KV_d^2)]} \quad (3)$$

$$I_2 = I_T/2 - ½V_d\sqrt{[K(2I_T - KV_d^2)]} \quad (4)$$

It can be seen from Eqs. (3 and 4) that each drain current is centered on $I_T/2$. Within a range, as V_d increases each drain current ramps up and down from $I_T/2$.

The differential output current $I_1 - I_2$ is represented by,

$$I_{out} = V_d\sqrt{[K(2I_T - KV_d^2)]} \quad (5)$$

If a diode connected device is added to each gate of differential pair, a highly linear current mode amplifier can be created. Linearity can be achieved across the full differential input range. The gate voltages are controlled by the currents forced across the diode connected devices according to following relation.

$$V_g = V_t + \sqrt{(I_d/K)} \quad (6)$$

Comparing to the single differential pair, the differential input voltage, V_d, now becomes

$$V_d = \sqrt{(I_{d1}/K)} - \sqrt{(I_{d2}/K)} \quad (7)$$

Adding and by solving the diode and current sources creates a new equation for I_{out}

$$I^2_{out} = I^2_{D1} - 2I_{D1}I_{D2} + I^2_{D2} \quad (8)$$

where, $I_{out} = (I_{D1} - I_{D2})$.

Combining two CMOS current mode amplifiers creates the CMOS multiplier. Defining the CMOS multiplier drain currents by these equations

$$I_1 = I_{T1}/2 + ½V_d\sqrt{[K(2I_{T1} - KV_d^2)]} \quad (9)$$

$$I_2 = I_{T1}/2 - ½V_d\sqrt{[K(2I_{T1} - KV_d^2)]} \quad (10)$$

$$I_3 = I_{T2}/2 + ½V_d\sqrt{[K(2I_{T2} - KV_d^2)]} \quad (11)$$

$$I_4 = I_{T2}/2 - ½V_d\sqrt{[K(2I_{T2} - KV_d^2)]} \quad (12)$$

Where all transistors are of the same size (same K) and $V_d = (V_{D1} - V_{D2})$. Currents sum at the outputs according to $I_{o1} = I_1 + I_3$ and $I_{o2} = I_2 + I_4$. The differential output current becomes $I_{out} = I_{o1} + I_{o2.}$ Since the multiplier is used as a differential pair squarer, V_m is grounded.

The squarer output relation is represented as,

$$V_o = K(V_c * V_s)$$

where K is the multiplication constant.

The second squarer circuit shown in Figure 4 consists of CMOS class AB amplifier [1] which is modified to receive the differential input current I_{in}. The current gain of the P-type current mirror $M_7 - M_8$ is unity. Neglecting the body effect and if all of the transistors are biased in saturation region, then the drain current equation is expressed as,

$$I_{DD} = I_{DD} - \tfrac{1}{2}I_{in} + I^2_{in}/16I_{DD} \quad (13)$$

$$I_{DD} = I_{DD} + \tfrac{1}{2}I_{in} + I^2_{in}/16I_{DD} \quad (14)$$

The summation of the drain currents I_{d3} and I_{d5} is copied by the p-type current mirror $M_7 - M_8$. Then the output current I_o can be written as,

$$Io = (I_{d3} + I_{dS}) - 2I_{DD} \quad \text{where}$$

$$I_o = I^2_{in}/16I_{DD} \text{ for } |I_{in}| \leq 4I_{DD} \quad (15)$$

It is clear that the output current I_o is related to the square of the input current I_{in}, where the squarer factor can be controlled by the bias current I_{DD}, as indicated by Eq. (15).

On the other hand, if bias current $I_{DD} < I_{in}/4$ then the circuit will operate in class B mode. It means that

$$I_o = I_{d5} = I_{in} \text{ for } I_{in} > 0$$

$$I_o = I_{d3} = I_{in} \text{ for } I_{in} < 0$$

Therefore, the output current becomes

$$I_o = |I_{in}| \quad (16)$$

In this case, the circuit represents a current full wave rectifier as shown in Figure 5.

4. DESIGN DETAILS

In the proposed architecture shown in Figure 6 of mixer with envelop detector, modulated signal is generated and fed to the input of rectifier. Signal is now retrieved at the output with the help of RC pair. In this case, the values of R and C are set as 1 kΩ and 11 nf respectively.

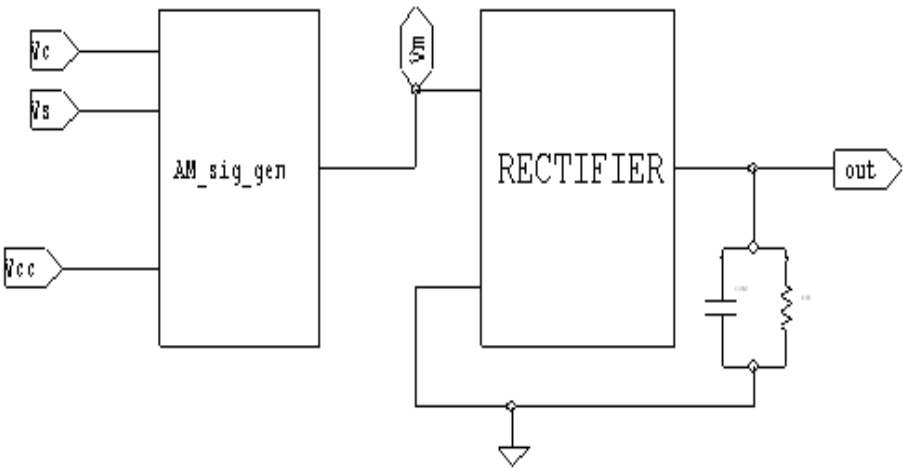

Fig. 6: *Mixer with Envelop Detector.*

Similarly, in Figure 7 for modem circuit type I, modulated signal generation and envelop detection is done in the same manner but a squarer is used before the rectifier. The squarer is shown in Figure 3. It is used to reduce the output noise and for a smooth response. This performs a better output in contrast with mixer with envelop detector which is presented in Figure 6.

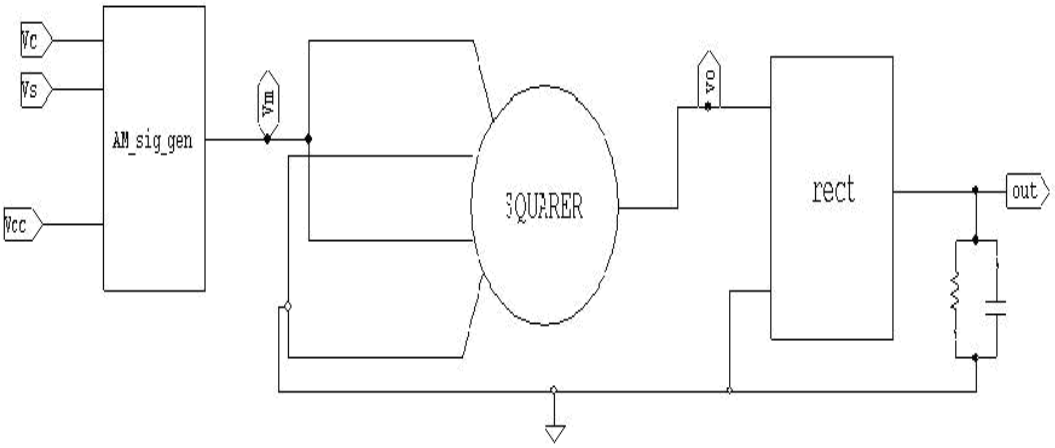

Fig. 7: *Modem Circuit Type I.*

Modem circuit type II shown in Figure 8 is used for the best performance among all three designs presented in this paper. In this module, the squarer circuit shown in Figure 3 is replaced by the squarer circuit presented in Figure 4 for better outputs.

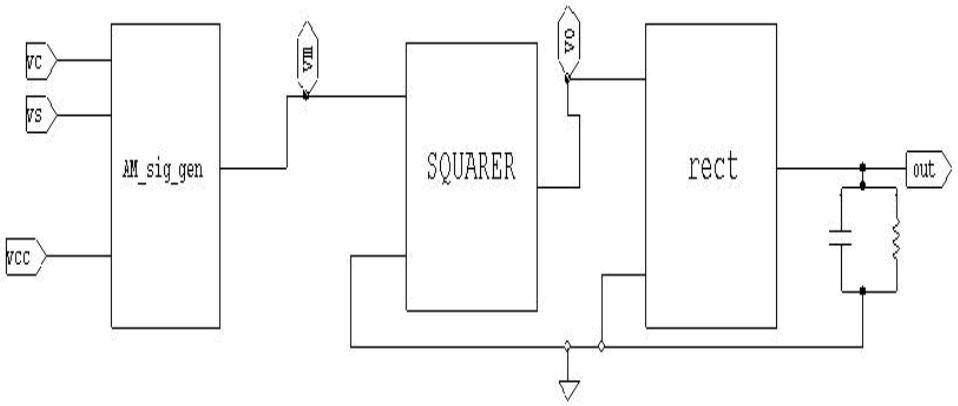

Fig. 8: *Modem Circuit Type II.*

5. SIMULATION RESULTS

Simulation results are shown in Table I for 500 mV signal and 1 V carrier for Type I and II schematics for different frequency ranges.

Table I:

f_{sig}/f_{car}	R & C	V_m (mod)	V_o (mult/ squ)	V_{out} Output for Type I/ Type II
18 kHz/200 MHz	10 kΩ & 470 pF	± 8m V ± 6m V	± 10 µV ± 5 mV	± 1 µV ± 150 µV
200KHz/2.4GHz	1k Ω & 800 pF	± 18 mV ± 60 mV	± 350 µV ± 6 mV	± 300 pV ± 60 µV
2MHz/2.4GHz	1 kΩ & 80 pF	± 20 mV ± 60 mV	± 350 µV ± 60 µV	± 35 pV ± 75 µV
20MHz/2.4GHz	1 kΩ & 8 pF	± 20 mV ± 60 mV	± 350 µV ± 60 µV	± 30 pV ± 75 µV

The proposed circuits of Figures 7 and 8 were simulated by Spice using the model parameter of SCL 1.2 µm CMOS process level 13.

The input audio signal of frequency 18 kHz and carrier signal of frequency 20 MHz were considered in Figures 9 and 10, V_m is modulated output (V_{mod}), V_o is the output of multiplier/squarer and V_{out} is the final output of the detector. Results in Figure 9 for modem of type I show that V_o and V_{out} are very low in range of mV and µV respectively while these are improved in Figure 10 for modem type II to mV ranges for V_o and V_{out}. Modem (TRX) response at 18 kHz Signal with 20 MHz carrier, for R = 10 kΩ and C = 470 pF.

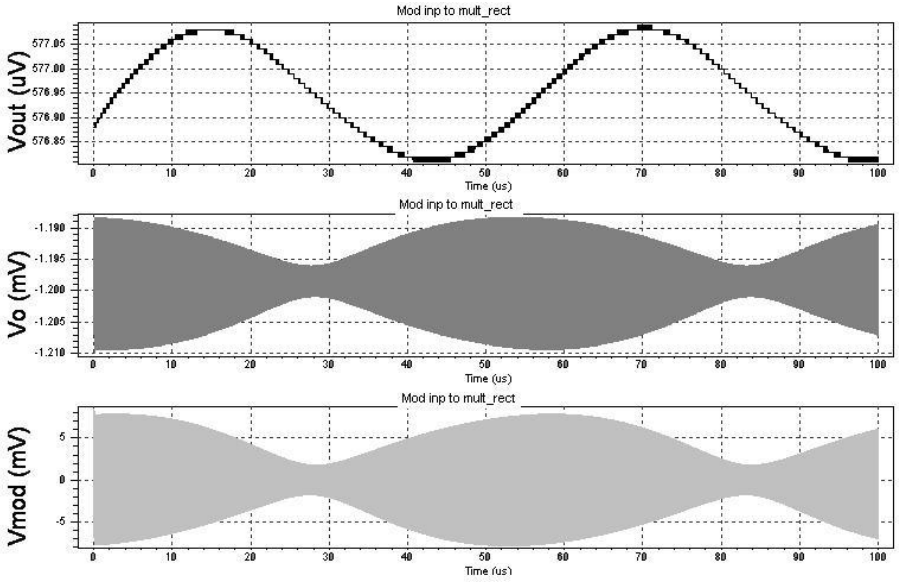

Fig. 9: *Simulated Response of TRX Type I.*

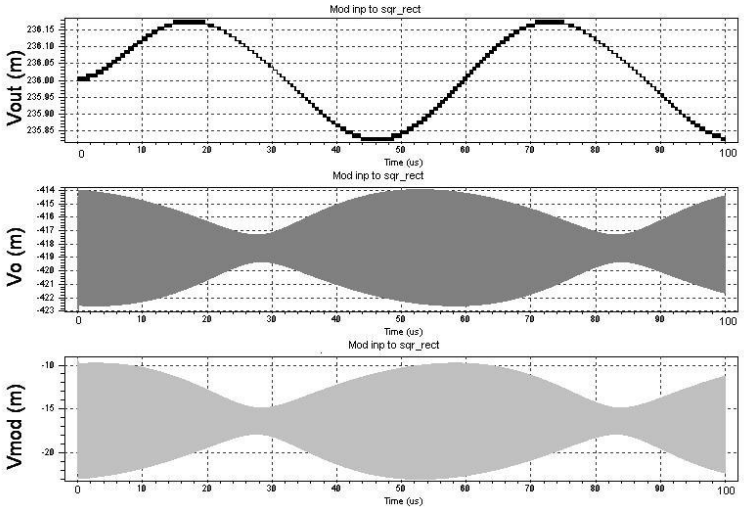

Fig. 10: *Simulated Response of TRX Type II.*

6. CONCLUSIONS

The design presented in this paper is compatible with the requirements of wireless sensors. The realization of the proposed circuit for modem is made up of AM modulator, multiplier/squarer and envelop detector. Here the squarer and rectifier circuits are based on the use of modified CMOS class AB amplifier. It requires low power CMOS power supplies where devices are functional in the saturation region (Square's law). The observed output signal at the receiver end is found in the same frequency range and in phase of the input signal generated either by the wireless sensor or other signal source to be transmitted after its modulation over carrier using wireless topology. The receiver is capable of detecting a low power modulated weak signal. The circuit can operate at supply voltage down to 5 V. The proposed circuit can be fully integrated with sensors, lowering the component count of the system and increasing its reliability.

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