

Time Domain Analysis in an On-chip High Speed RLCG Interconnection Network at 0.18 μm Technology

Vikas Maheshwari¹, Abhishek Sharma², Rajib Kar³, Durbadal Mandal³, A.K. Bhattacharjee⁴

¹Deptt. of ECE, Anand Engineering College, Agara, U.P., India

²Deptt. of ECE, Hindustan College of Science and Technology, Mathura, U.P., India

³Deptt. of ECE, National Institute of Technology, Durgapur, West Bengal, India

ABSTRACT

In this model, the time domain waveform is evaluated for calculation of delay time, peak time, settling time, damping ratio and natural frequency for a second order RLCG interconnect network. It can also be used for multiple interconnect systems but for higher order systems it is ignored due to accurate analysis. The model is applied to a single resistance-inductance-capacitance-conductance model which can also be extended to multi-interconnect systems to analyze the rise time and settling time in similar analysis. The model evaluates the performance of a system which is expressed in terms of the transient response for the unit impulse input because it is easy to generate and evaluate the delay analytically. The transient response of a system to a unit impulse input depends upon the initial conditions. In this paper, a new interconnect model is presented; the model is based on the RLCG transmission line whose response is evaluated in time domain for a unit impulse input. In this model the delay is calculated in SPICE and MATLAB. No approximation is made to the transfer function of the interconnect. A closed form expression for the propagation delay of a CMOS gate driving a distributed RLCG line is introduced. On-chip inductance and conductance are shown to have a profound effect on the high performance IC design methodologies. In this proposed model we have shown that with the increase in the value of conductance by keeping constant the values of R, L, C we evaluate that the SPICE delay reduces but if we compare it with the MATLAB proposed delay model we see very accurately that the variation in the proposed delay is much larger in comparison to the SPICE delay. Hence, for a high-speed circuit, one must increase the value of G, so that the steady-state condition is reached as soon as possible. The simulation results performed in Cadence SPICE environment justify the efficiency of the proposed model.

Keywords: Time domain analysis, damping ratio, natural frequency, delay calculation, RLCG interconnect, VLSI

***Authors for Correspondence** Email: abhi10091986@gmail.com, maheshwari_vikas1982@yahoo.com, rajibkarece@gmail.com

INTRODUCTION

The design techniques in sub-micron technologies result in the effects of coupling in interconnections [1]. Indeed, in technologies greatly in sub-micron, the order of coupling between lines reach some severe values so that we cannot be indifferent to the amplexness of the noise due to this coupling [2]. As integrated circuit feature sizes continue to scale well below 0.18 microns, active device counts are reaching hundreds of millions [3]. The amount of interconnect among the devices tends to grow

super linearly with the transistor counts, and the chip area is often limited by the physical interconnect [21] area. Several factors bound to the technology contribute to the bandwidth problems. Bandwidth has a key role in the performance of any circuit basically used for data transmitting applications. A higher bandwidth reduces the total time required to transmit a certain amount of data, thereby increasing the performance of the system. Global communication architecture based on a global mesochronous, local synchronous approach allows very high data rate per wire and therefore

very high bandwidth in buses of limited width. This set of new challenges is referred to as signal integrity in general. Among all these problems, capacitive coupling induced cross talk is the issue that has been observed by an increasing number of backend vendors. Delay is determined by considering the time domain analysis on a transmission line after applying the input at how much delay the output is being obtained. Especially for an on-chip bus, delay is a serious problem for VLSI design. In bus structure, delay is most important because long interconnect [14] wires often run together and in parallel. Interconnect [15] lines may be coupled to study the effects of mutual inductive and capacitive coupling, such as delay. It is possible to use both a distributed and a lumped model for these macro models. Pole [20] zero analysis is also being evaluated for finding the stability of the system.

The rest of the paper is organized as follows: Section 2 discusses the basic theory, transmission line model, crosstalk, glitch and different modes of operation. Section 3 describes the difference model approach and the proposed closed form formula for bandwidth. Section 4 shows the simulation results. Finally, section 5 concludes the paper.

BASIC THEORY

Transmission Line Models

Defining the point at which an interconnect should be treated as a transmission line and hence reflection analysis applied has no consensus of opinion. A rule of thumb is when

the delay [17] from one end to the other is greater than risetime/2, the line is considered electrically long. If the delay is less than risetime/2, the line is electrically short.

A transmission line [5] can be described at the circuit level using series inductance and resistance combined with shunt capacitance and conductance. An infinitesimal unit length of the transmission line looks like the circuit [19] in Figure 1. In Figure 1,

- R = Series resistance per unit length
- L = Series inductance per unit length
- G = Shunt conductance per unit length
- C = Shunt capacitance per unit length.

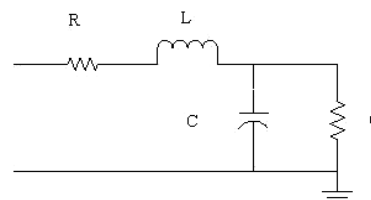


Fig. 1 RLCG Parameters for a Segment of a Transmission Line.

It is critical to model the transmission path when designing a high-performance, high-speed serial interconnect system. The transmission path may include long transmission lines, connectors, vias and crosstalk from adjacent interconnect. Values for R, L, C, and G are extracted from a given geometry in 0.13 micron technology.

Cross Talk

Crosstalk [13] is defined as the energy imparted to a transmission line due to signals [23] in adjacent lines. The magnitude of the crosstalk

induced is a function of risetime, signal line geometry and net configuration (type of terminations, etc.). In order to overcome the problems faced at high frequency of operation, shielding techniques have been employed [11]. A common method of shielding is placing ground or power lines at the sides of a victim signal line to reduce noise and delay uncertainty. The crosstalk between two coupled interconnects is often neglected when a shield is inserted, significantly underestimating the coupling noise. The crosstalk noise between two shielded interconnects can produce a peak noise of 15% of V_{DD} in a 0.18 μm CMOS technology [12]. An accurate estimate of the peak noise for shielded interconnects is therefore crucial for high performance VLSI design. In the complicated multilayered interconnect system, signal coupling and delay strongly affect circuit performances. Thus, accurate interconnect characterization and modeling are essential for today's VLSI circuit design. Two major impacts of cross talk are:

- (i) Crosstalk induces delays, which change the signal propagation time [18], and thus may lead to setup or hold time failures.
- (ii) Crosstalk induces glitches, which may cause voltage spikes on wire, resulting in false logic behavior. Crosstalk affects mutual inductance as well as inter-wire capacitance.

When the connectors in high-speed digital designs are considered, the mutual inductance plays a predominant role compared to the inter-wire capacitance. The effect of mutual inductance is significant in deep submicron (DSM) technology [4] since the spacing between

two adjacent bus lines is very small. The mutual inductance induces a current from an aggressor line onto a victim line which causes crosstalk between connector lines.

In multi-conductor systems, crosstalk can cause two detrimental effects: first, crosstalk will change the performance of the transmission lines in a bus by modifying the effective characteristic impedance and propagation velocity. Second, crosstalk [8] will induce noise onto other lines, which may further degrade the signal integrity and reduce noise margins.

Glitch

Crosstalk glitch (CTG) is a glitch signal provoked by coupling effects among interconnect lines which have unbalanced drivers and loads [6]. The magnitude of the glitch depends on the ratio of coupling capacitance between line to ground capacitance. When a transition signal is applied at a line which has a strong line-driver while stable signals are applied at other lines which have weaker drivers, the stable signals may experience a coupling noise due to the transition of the stronger signal. A glitch may be induced in connector "j" in which the signal is static, due to neighboring connector lines in which the signal is varying [7]. This is given by Eq. (1).

$$V_{glitch}^j = \sum_j \pm L_{jk} \frac{dj_k}{dt} \quad \forall j \neq k \quad (1)$$

where L_{jk} represents mutual inductance between j^{th} and k^{th} connector. The sign of the coupled voltage is positive or negative depending upon

whether the k^{th} neighboring connector undergoes a rising or a falling transition.

Odd Mode

When two coupled transmission lines are driven with voltages of equal magnitude and 180 degree out of phase with each other, odd mode propagation occurs. The effective capacitance of the transmission line will increase by twice the mutual capacitance, and the equivalent inductance will decrease by the mutual inductance. In Figure 2, a typical transmission line model is considered where the mutual inductance between aggressor and victim connector is represented as M_{12} , L_1 and L_2 represent the self inductances of aggressor and victim nodes while C_c , C , denote the coupling capacitance between aggressor and victim, self capacitance, respectively.

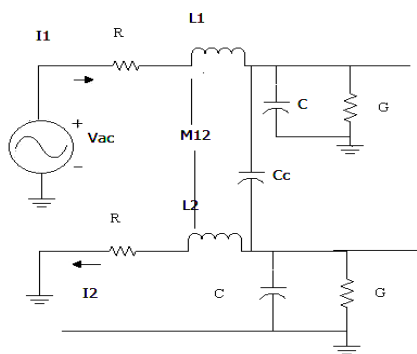


Fig. 2 An Example for Two Line Transmission Line Model.

Assuming that $L_1 = L_2 = L_0$, the currents will be of equal magnitude but will flow in opposite direction [7]. Thus, the effective inductance due to odd-mode of propagation is given by Eq. (2).

$$L_{\text{odd}} = L_1 - L_2 \quad (2)$$

The magnetic field pattern of the two conductors in odd-mode is shown in Figure 3.

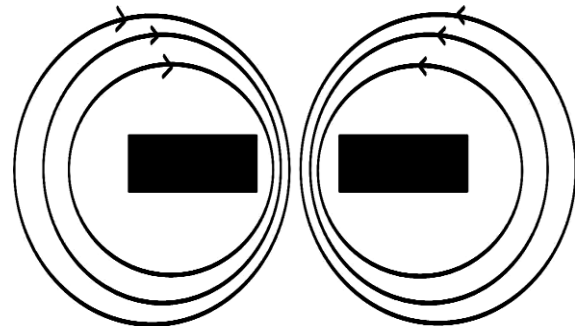


Fig. 3 Magnetic Field in Odd Mode.

Even Mode

When two coupled transmission lines are driven with voltages of equal magnitude and in phase with each other, even mode of propagation occurs. In this case, the effective capacitance of the transmission line will decrease by the mutual capacitance and the equivalent inductance will be increased by the mutual inductance. Thus, in even-mode of propagation, the currents will be of equal magnitude and flow in the same direction (Figure 4) [7]. The effective inductance, due to even mode of propagation is then given by Eq. (3).

$$L_{\text{even}} = L_1 + L_2 \quad (3)$$

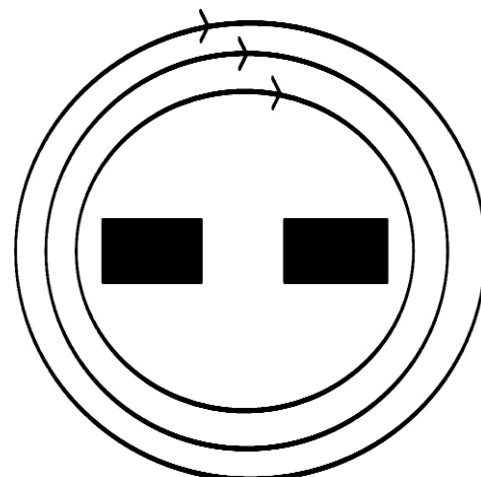


Fig. 4 Magnetic Field in Even Mode.

IMPULSE FUNCTION

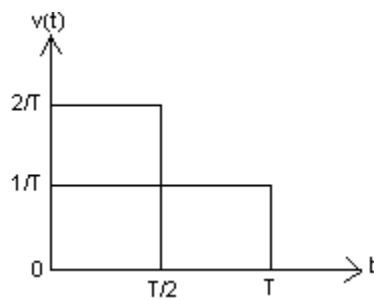


Fig. 5. Impulse Response Representation.

In Figure 2, the first pulse has a width T and a height of $1/T$ such that the area of the pulse is $T \times 1/T = 1$. If we halve the duration and double the amplitude we get the second pulse. The area under the second pulse is also unity. Note that the duration of the pulse approaches infinity but the area of the pulse is unity. The pulse for which the duration tends to zero and amplitude tends to infinity is called impulse function. Impulse function is also known as delta function, A unit impulse can be defined as,

$$\delta(t) = \begin{cases} 0 & ; t \neq 0 \\ \infty & ; t = 0 \end{cases}$$

(A)

MODELING OF CROSSTALK IN RLCG INTERCONNECT

Difference Model

The frequency-domain [25] difference approximation [10] procedure is more general, because it can directly handle lines with arbitrary frequency-dependent parameters or lines characterized by data measured in frequency-domain. The time-domain difference

approximation procedure should be employed only if transient characteristics are available. For a single RLCG line, the analytical expressions are obtained for the transient characteristics and limiting values for all the modules of the system and device models. The difference approximation procedure is applied to both the characteristic admittances and propagation functions and the resulting time-domain device models have the same form as the frequency-domain models.

The difference approximation procedure involves an approximation of the dynamic part of the system transfer function, given by Eq. (12), with the complex rational series or distorted part of the transient characteristic with the real exponential series. This criterion results in simple and efficient approximation algorithms, and requires a minimal number of the original-function samples to be available, which is important if the line is characterized with delay [9] and crosstalk aware bandwidth.

Modeling the Bandwidth Using Difference Model

We first consider the interconnect system consisting of single uniform line and ground as shown in Figure 5, and assume the length of the line is d .

A differential length of a line is assumed to possess distributed series inductance L and resistance R , as well as shunt capacitance C and conductance G . Kirchoff's law is assumed to hold for the small length (Figure 6).

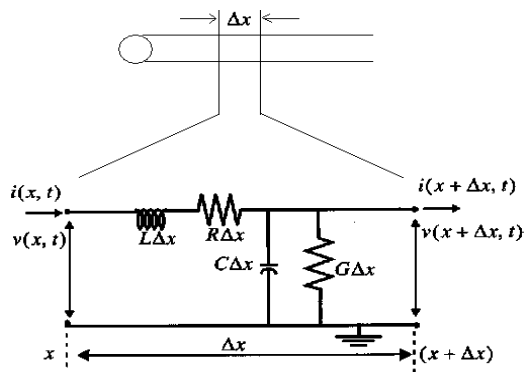


Fig. 6 Equivalent Circuit of Each Uniform Section.

The electrical parameters of each section are $R_{\Delta x}$, $L_{\Delta x}$, $C_{\Delta x}$ and $G_{\Delta x}$, respectively, where R , L , C and G are per-unit length resistance, inductance, capacitance and conductance of the line.

Using Kirchoff's voltage law, we can write,

$$v(x, t) = i(x, t)R_{\Delta x} + L_{\Delta x} \frac{di(x, t)}{dt} + v(x + \Delta x, t) \quad (4)$$

Using Kirchoff's current law, we can write,

$$i(x, t) = G_{\Delta x}v(x + \Delta x, t) + C_{\Delta x} \frac{dv(x + \Delta x, t)}{dt} + i(x + \Delta x, t) \quad (5)$$

Simplifying the above two equations and applying Laplace transformation, we get,

$$-\frac{\partial V(x)}{\partial x} = (R + sL)I(x) \quad (6)$$

$$-\frac{\partial I(x)}{\partial x} = (G + sC)V(x) \quad (7)$$

Differentiating Eqs. (6) and (7) with respect to x , and after simplifying we get,

$$\frac{\partial^2 V(x)}{\partial x^2} = P^2 V(x) \quad (8)$$

And

$$\frac{\partial^2 I(x)}{\partial x^2} = P^2 I(x) \quad (9)$$

where P is the propagation constant and is defined as,

$$Pd = \sqrt{(R + sL)(G + sC)}$$

The general solution of Eq. (8) is given by,

$$V(x) = A_1 e^{-Px} + A_2 e^{Px} \quad (10)$$

Where A_1 and A_2 are the constants determined by the boundary conditions. From Eqs. (8) and (10), we get,

$$-\frac{\partial}{\partial x} [A_1 e^{-Px} + A_2 e^{Px}] = (R + sL)I(x)$$

After simplifying we get,

$$I(x) = \frac{1}{Z_0} [A_1 e^{-Px} - A_2 e^{Px}] \quad (11)$$

where Z_0 is the characteristic impedance.

Assuming that $x = d$, the termination voltage and current are $V(d) = V_2$ and $I(d) = I_2$, respectively, then we get,

$$V_2 = A_1 e^{-Pd} + A_2 e^{Pd} \quad (12)$$

$$I_2 = \frac{1}{Z_0} [A_1 e^{-Pd} - A_2 e^{Pd}] \quad (13)$$

From Eqs. (12) and (13) we get,

$$A_1 = \frac{1}{2} [V_2 + I_2 Z_0] e^{Pd}$$

$$A_2 = \frac{1}{2} [V_2 - I_2 Z_0] e^{-Pd}$$

Substituting these values of A_1 and A_2 in Eq. (10)

$$V(x) = \left[\frac{[V_2 + I_2 Z_0]}{2} e^{P(d-x)} + \frac{[V_2 - I_2 Z_0]}{2} e^{P(x-d)} \right] \quad (14)$$

Similarly we calculate for $I(x)$ as,

$$I(x) = \frac{1}{Z_0} \left[\frac{[V_2 + I_2 Z_0]}{2} e^{P(d-x)} - \frac{[V_2 - I_2 Z_0]}{2} e^{P(x-d)} \right] \quad (15)$$

Let at $x = 0$, $V(x) = V_1$ and $I(x) = I_1$ then from Eqs. (12) and (14), we can write,

$$V_1 = \cosh(Pd)V_2 + Z_0 \sinh(Pd)I_2 \quad (16)$$

$$I_1 = \frac{1}{Z_0} \sinh(Pd)V_2 + \cosh(Pd)I_2 \quad (17)$$

Since ABCD parameters are defined as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

So we can write ABCD matrix from Eqs. (16) and (17)

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cosh(Pd) & -Z_0 \sinh(Pd) \\ \frac{1}{Z_0} \sinh(Pd) & -\cosh(Pd) \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (18)$$

The output crosstalk voltage is given by,

$$V_2(s) = \frac{V_1(s)}{\cosh(Pd)} \quad (19)$$

From Eq. (19), we can write the equation for the transfer function of the system

$$H(s) = \frac{V_2(s)}{V_1(s)} = \frac{1}{\cosh(Pd)} \quad (20)$$

After simplification of Eq. (20), we get the open loop transfer function,

$$G(s) = \frac{V_2(s)}{V_1(s)} = \frac{1}{\left(s + \frac{R}{L}\right)\left(s + \frac{G}{C}\right)} \quad (21)$$

The above equation can be written as,

$$G(s) = \frac{V_2(s)}{V_1(s)} = \frac{1}{\left\{s^2 + s\left(\frac{LG + RC}{LC}\right) + \frac{RG}{LC}\right\}} \quad (22)$$

For the stability analysis of the control system, we must find out the closed loop transfer function by considering the unity feed back with unit step input.

Consider the time response of second order [22] system, in which we consider the general form of closed loop transfer function which can be written as,

$$C(s) = \frac{V_2}{V_1} = \frac{G(s)}{1 + G(s)H(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (23)$$

where ω_n and ζ are the natural frequency and damping ratio.

So the characteristic equation for this transfer function can be written as,

$$1 + G(s)H(s) = 0 \quad (24)$$

By considering the open loop transfer function with unity feed back, Eq. (22) can be written as,

$$G(s) = \frac{V_2(s)}{V_1(s)} = \frac{1}{\left\{s^2 + s\left(\frac{LG + RC}{LC}\right) + \left(\frac{RG}{LC} + 1\right)\right\}} \quad (25)$$

For unity feedback and the unit impulse input, the above equation can be written as,

$$1 + G(s) = 0 \quad (26)$$

Now by using Eq. (24) the characteristic equation can be written as,

$$s^2 + s\left(\frac{LG + RC}{LC}\right) + \left(\frac{RG}{LC} + 1\right) = 0 \quad (27)$$

Now comparing the characteristic equation of second order system with unity feedback Eq. (27), we obtain the values of ω_n and ζ which are the natural frequency and damping ratios (Figure 7).

$$\omega_n = \sqrt{\frac{RG + 1}{LC}} \quad (28)$$

$$\zeta = \frac{\frac{RC + LG}{LC}}{\sqrt{\left(1 + \frac{RG}{LC}\right)}} \quad (29)$$

$$\tau_d = \frac{\tau_{plh} + \tau_{phl}}{2} \quad (30)$$

$$\tau_{PHL} = \frac{C_{load}}{K_n(V_{DD} - V_{T,n})} \left[\frac{2V_{T,n}}{(V_{DD} - V_{T,n})} + \ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1\right) \right] \quad (31)$$

$$\text{where } K_n = \mu_n \cdot C_{OX} \left(\frac{W_n}{L_n} \right) \quad (32)$$

$$\tau_{PHL} = \frac{C_{load}}{K_p(V_{DD} - |V_{T,p}|)} \left[\frac{2|V_{T,p}|}{(V_{DD} - |V_{T,p}|)} + \ln\left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1\right) \right] \quad (33)$$

$$\text{where } K_p = \mu_p \cdot C_{OX} \left(\frac{W_p}{L_p} \right) \quad (34)$$

C_{load} : Capacitive load applied to the output of the inverter

C_{OX} : Gate-oxide capacitance

V_T : Threshold voltage for a transistor

V_{DD} : Drain voltage applied to PMOS drain terminal.

μ_p, μ_n : Mobility of electrons and holes through transistor channel.

K_n, K_p : Transconductance of the NMOS and PMOS transistors

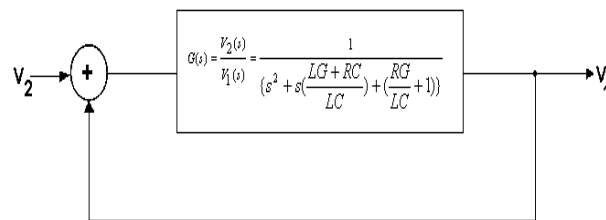


Fig.7 Bloch Diagram of a Second Order System.

EXPERIMENTAL RESULTS

Most of the earlier research and reduction techniques consider only capacitive coupling. But in the case of very high frequencies as in GHz scale, inductive crosstalk comes into the important role and it should be included for complete coupling noise analysis. The configuration of circuit for simulation [24] is shown in Figure 2. The high-speed interconnect

system consists of two coupled interconnect lines and ground and the length of the lines is $d = 10$ mm. The sample dimensions of the cross sections of a minimum-sized wire in a $0.18 \mu\text{m}$ technology are given in Figure 8.

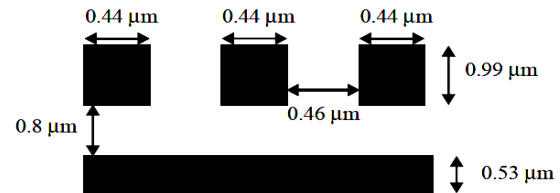


Fig. 8 Sample Dimensions of Cross Sections of Minimum-Sized Wire in a $0.18 \mu\text{m}$ Technology. The extracted values for the parameters R, L, C, and G are given in Table I.

Table I RLCG Parameters for a Minimum-Sized wire in a $0.18 \mu\text{m}$ Technology, Where the Conductance is a Function of Frequency, F.

Parameter(s)	Value/m
Resistance(R)	120 kΩ/m
Inductance(L)	270 nH/m
Conductance(G)	15 fpS/m
Capacitance(C)	240 pF/m

Table II RLCG Parameters for a Minimum-Sized Wire in a $0.18 \mu\text{m}$ Technology and the Delay Model Parameters.

R (KΩ)	L (nH)	C (pF)	G (ms)	ω_n rad/s (10^{10})	ζ	SPICE delay [td(ns)]	Proposed delay [td(ns)]
1.2	2.7	2.4	1.5	1.66	26.81	1.46	27.25
1.2	2.7	2.4	2.25	2.03	26.83	3.99	24.35
1.2	2.7	2.4	3	2.35	26.84	2.58	21.00
1.2	2.7	2.4	3.725	2.62	26.86	0.68	18.85

In Table II we evaluate the performance of the system by calculating the values of ω_n natural frequency ζ damping ratio at that frequency. We calculate the MATLAB delay model for evaluation of time-domain analysis by using Eqs. (28) and (29). In this proposed model we see that with the increase in the value of conductance by keeping constant the values of R, L, C we evaluate that the SPICE [16] delay reduces but if we compare it with the MATLAB proposed delay model we see very accurately that the variation in the proposed delay is much larger as compared to the SPICE delay.

In Table III we have shown that with the increase in the value of G the amplitude of the impulse response increases and also the time of that amplitude also increases but the settling time reduces.

In Table III, peak time is the time required for the response to reach the first peak of the time response or the first peak overshoot, and the settling time is the time required for the response to reach and stay within the specified range (2% to 5%) of its final value.

Table III. RLCG Parameters for a Minimum-Sized Wire in a 0.18 μm Technology and the Time Domain Analysis Parameters.

R (K Ω)	L (nH)	C (pF)	G (mS)	Peak Amplitude Time (t_p (ns))	Settling Time (t_s (ns))
1.2	2.7	2.4	1.5	0.30	0.12
1.2	2.7	2.4	2.25	0.37	0.10
1.2	2.7	2.4	3	0.43	0.89
1.2	2.7	2.4	3.725	0.47	0.80

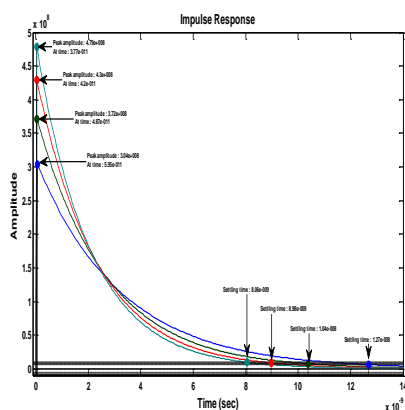


Fig. 9 Impulse Response of a Linear Time Invariant System.

In Figure 9, we have shown that with the increase in the value of G the peak amplitude of the impulse response increases and the time to reach the peak amplitude increases, similarly settling time also reduces. In Figure 9, we do not vary the value of R, L, C but vary the value of G in which we evaluate the performance of transmission line with the dependence of conductance (Figures 10–13).

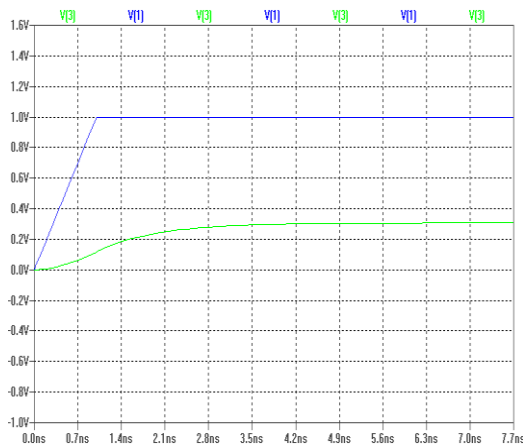


Fig. 10 A Spice Model for Delay Calculation in RLCG Network for the Values $R(K\Omega) = 1.2$, $L(nH) = 2.7$, $C(pF) = 2.4$ and $G(mS) = 1.5$ in a $0.18 \mu m$ technology.

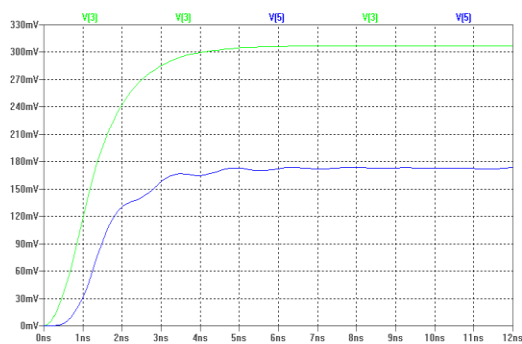


Fig. 11 A Spice Model for Delay Calculation in RLCG Network Using Values $R(K\Omega) = 1.2$, $L(nH) = 2.7$, $C(pF) = 2.4$ and $G(mS) = 2.25$ in a $0.18 \mu m$ technology.



Fig. 12 A Spice Model for Delay Calculation in RLCG Network Using Values $R(K\Omega) = 1.2$, $L(nH) = 2.7$, $C(pF) = 2.4$ and $G(mS) = 3.0$ in a $0.18 \mu m$ Technology.

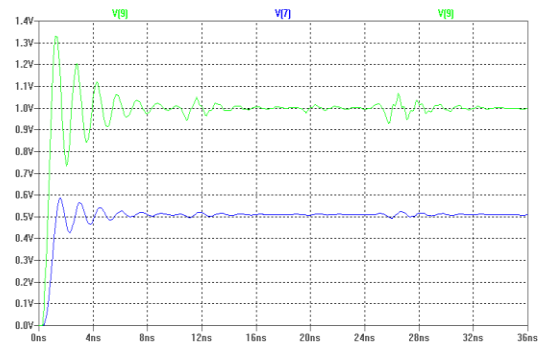


Fig. 13 A Spice Model for Delay Calculation in RLCG Network Using Values $R(K\Omega) = 1.2$, $L(nH) = 2.7$, $C(pF) = 2.4$ and $G(mS) = 3.725$ in a $0.18 \mu m$ Technology.

CONCLUSIONS

In this paper, we have proposed an efficient as well as accurate model for delay estimation for on-chip VLSI interconnect. We have derived damping ratio and natural frequency for evaluation of delay into consideration. We have modeled the on-chip interconnect as a distributed RLCG transmission line. We evaluate the performance interconnection network by time-domain analysis.

REFERENCES

1. L. Gal. *IEEE Custom Integrated Circuits Conference*. 1995. 251–254p.
2. *National Technology Roadmap for semiconductors*. Semiconductor Industry Association. 1997.
3. Shien-Yang Wu, Boon-Khim Liew, K.L. Young, et al. *IEEE International Conference Interconnect Technology*. May 1999. 68–70p.

4. S. Delmas-Bendhia, F. Caignet, E. Sicard. *IEEE International Caracas Conference on Devices, Circuits and Systems*. 2000.
5. Saihua Lin, Huazhong Yang *IEEE Transactions on Computer-Aided Design of Integral Circuit Systems*. 2006.
6. K. Lee, C. Nordquist, J. Abraham. *IEEE International Symposium on Circuits and Systems*. 1996. 4. 628–631p.
7. Clayton R. Paul, Keith W. Whites, Syed A. et al. *Introduction to Electromagnetic Fields*. McGraw Hill. 1998.
8. J.V.R. Ravindra, M.B. Srinivas *Proceedings of the 20th Annual Conference on Integrated Circuits and Systems Design*. 2007. 207–211p.
9. Y. Gao and D. F. Wong. *Proceedings of International Conference On Computer-Aided Design (ICCAD)*. 1998. 611–616p.
10. D.B. Kuznetsov and J. E. Schutt-Aine. *IEEE Transactions on Circuits and Systems I*. Feb. 1996. 43. 110–121p..
11. J. Zhang and E. G. Friedman. *Proceeding of the IEEE International Symposium on Circuit and Systems*, May 2004. 2. 529–532p.
12. Y. Massoud, J. Kawa, D. MacMillen. et al. *IEEE/ACM DAC 2001*. Las Vegas, Nevada, USA. June 18–22, 2001.
13. A. Vittal, M. and Marek-Sadowska. *IEEE Transactions on Computer-Aided Design*. Mar. 1997. 16. 290–298p.
14. A. Vittal, L. H. Chen, M. Marek-Sadowska. *IEEE Transactions on Computer-Aided Design*. 1999. 18(12). 1817–1824p.
15. A. Devgan. *IEEE Proceedings ICCAD*. Nov. 1997. 147–153p.
16. *Star-HSPICE Manual*. Avanti Corp. 1999.
17. C. J. Alpert, A. Devgan, S. T. Quay. *IEEE Transactions on Computer-Aided Design*. 1999. 18(11). 1633–1645p.
18. L. T. Pillage and R. A. Rohrer. *IEEE Transactions on Computer-Aided Design*. Apr. 1990. 9. 352–366p.
19. P. Feldmann and R. W. Freund. *IEEE Transactions on Computer-Aided Design*. 1995. 14. 639–649p.
20. K. J. Kerns and A. T. Yang. *IEEE Transactions on Computer-Aided Design*. 1997. 16.
21. A. Odabasioglu, M. Celik, L. T. Pileggi. *IEEE Transactions on Computer-Aided Design*. 1998. 17(8). 645–654p.
22. P. Rabiei and M. Pedram. *IEEE Proceedings ASP-DAC*. 1999.
23. M. Shimanouchi *Proceedings of ITC International Test Conference*. 2002. 903–912p.
24. K. Helmreich. *Proceedings of ITC International Test Conference*. 2001. 415–423p.
25. U. Schoettmer C. Wagner, T. Bleakley. *Proceedings of ITC International Test Conference*. 2000. 995–1004p.