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Performance Analysis of 3T DRAM Using FinFET Based with Leakage Reduction Techniques at 45 nm Technology

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Abstract

The proposed area of research is to reduce the power consumption, leakage voltage, leakage current and leakage power of DRAM while maintaining the competitive performance. The Fin FET approach is used in DRAM for high performance. Fin type field effect transistors (Fin FET) are capable substitutes for bulk CMOS at the nano-scale. Fin FET are double gate device. A Fin FET uses an intrinsic body. It greatly suppresses the device-performance variability caused by the fluctuation in the number of dopant ions, while a planar-bulk MOSFET requires a heavily doped channel which causes serious process variability. A Fin FET based DRAM memory design has been proposed as an alternative solution to the bulk devices. Fin FET is suitable for future nano-scale memory circuit design due to its reduced short channel effects (SCE) and leakage current. Fin FET DRAM cells can reduce area and leakage power. Z` `By using the Fin FET CMOS technology we investigate that it provide low leakage and high performance operation by utilizing high speed, low Vt transistor for logic cell and low leakage.

Keywords: *DRAM, Fin FET, CMOS, Leakage power, Leakage current*

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INTRODUCTION

Semiconductor memories are most important microelectronic component of digital logic system design whose application is based on microprocessor and computer which ranging from satellite to consumer electronics. The amount of memory required is mainly depend on the significance of device and importance of transistor because storing function require more number of transistor as compare to logic operation. Memory array that are placed on chip have been extensively in sub-system of VLSI circuit and economically available single chip read/write memory capacity has grasped 1 GB of amount [1, 2]. The properties of semiconductor based memory are its random accessing that indicates accessing of data from any location in the memory so that data can be accessed fast in random manner. The access time of semiconductor memory is much faster than other type of data storage; within few nanoseconds a byte of data can read or written. Memory cell consisting of one to several transistor are there in semiconductor memory where each bit of binary data is stored. On the basis of stored data and accessed data the semiconductor memory is generally catalogued. In RAM the modification of input bits stored in memory array is permitted [3, 6]. The storage is volatile, i.e. when power is turned off the stored data is lost. In modern age we commonly use the term “memory” to refer to RAM in electronic industry. RAM is used to hold instruction temporarily and necessary data for CPU (central processing unit) to process task. To buffer a various type off information in networking equipment memory is used. On the basis of the functionality of storing individual data, RAM’s are classified in to two main categories: dynamic RAM (DRAM) [7–13] and static RAM (SRAM) [2–6].

The SRAM do not need refreshing operation as it consists of latch to keep the stored data as long as power is turned on. In DRAM binary information is stored in capacitor which is access by the transistor. At the storage node the junction leakage current degrades the mostly cell information. The cell data is

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therefore read and rewritten periodically even when the memory array is not accessed. Presented paper is prepared in such a manner as in the dynamic memory technology which is described along with the initial development as well as fundamental concepts. Further, the paper explains about the operational functions like read and write operations of the conventional DRAM. Then the evolution of DGF in FET based design over the conventional MOSFET based 3T DRAM. After that, the paper explains the major leakage reduction approach, i.e. SVL along with the sub modules knows as USVL and LSVL with simulation table and performance graphs. Lastly described is the conclusion of the performed research.

DYNAMIC MEMORY TECHNOLOGY

DRAM devices are most commonly used in various electronics application where speed is not the main factor. DRAMs are mainly used in main memory because of its simple circuitry, less complex design and low cost, it is the first choice of designer for the purpose of microprocessor bade system. Even though these devices are available in various sizes, scales and marketed in a different kind of wide verity of packages, their overall functionality is essentially the same. For the sole purpose of data storage DRAMs are basically designed. Storing data in device, reading the data stored in device and periodically refreshing the data is the only valid operation on a memory device. Various methodologies for writing and reading the memory have been developed to improve efficiency and speed. Synchronous DRAM and asynchronous DRAM are same in many aspect; clocked interface and multiple bank architecture is used in synchronous operation. DRAM chip are the array of memory cells, which are large in size and rectangular in shape with logic circuit which support DRAM for the purpose of reading from and writing in the array. It also consists of element that provides refreshing to maintain the data stored to have significant integrity of data. In memory cell the memory arrays are structured in rows called word line and columns called bit line. Each of the memory cells has distinct architecture or can be said as address which is recognized by the intersection points of particularly row and column.

The first DRAM of 1 kb capacity was proposed in 1970, since then DRAMs have been the major driving force behind VLSI technology development. The DRAM capacity has increased six times in last 3 decades from the one 1 kb in 1970 to 1-to-4 Gb level today, It consist of a capacitor that perform the action of continuous charges or discharges to produce a 1 (HIGH) or a 0 (LOW). Over the years, many more different structures have been designed to create the memory cells on a single chip. In today's methodologies, nano-scale trenches are filled with the fine dielectric material which is used to create the capacitive storage element for the memory cell.

READ/WRITE OPERATION OF 3T DRAM CELL

In 3T DRAM, a single transistor T2 is used as a storage device out of 3 transistors and its operation of ON and OFF state depend on charged stored in the gate capacitance. Read and Write is accessed by one transistor each. Write operation is performed only when the word line is enabled (high state or logic high) and the bit line is transferred on to the gate terminal of storing device through transistor T1 as a voltage whereas during read operation voltage is discharge to ground through T2 and T3 transistor, when the voltage applied to the gate of storing devices is high. When the word line is made disabled (low state or logic level low) the circuit is neither in the read or write operation mode rather it goes to hold state. The advantage of 3T DRAM is that read operation is relatively fast and non-destructive with the trade of large cell due to four lines (two bit line and two word line) (Figure 1).

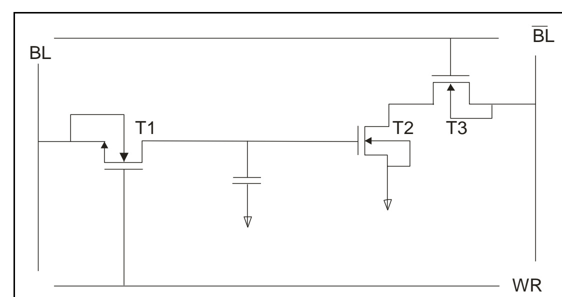

Fig. 1: *Conventional 3T DRAM Circuit.*

3T DRAM USING FINFET TECHNOLOGY

The word FinFET was coined for the University of California, Berkley researchers (Profs. Chenminghu, Tsu-Jae King-Liu and Jeffrey Bokor) to explain the concept of a non-planar Double-Gate transistor built on a SOI Substrate based on the previous DELTA (Single-gate) transistor design. The discriminating behavior of the FinFET is its conducting channel that is covered by a thin silicon film called "Fin", which forms the main body of the device. The dimension of the fin (considered in the direction from source to drain) depicts the practical length of the device. We are proposing a 3T DRAM by using FinFET technique for reducing the leakage power, leakage current and leakage voltage with 45 nm process technology. FinFET 3T DRAM have appeared as an upcoming replacement for conventional 3T DRAM at the 45 nm node and surpassing.

FinFET is a non-planar double gate device, which implement strict control of SCEs, decrease sub threshold leakage, and better stability. FinFET also cover less area because fin height estimate effective channel width [15]. FinFET based 3T DRAM has the advantage of low leakage power and dynamic power. The proposed design has been verified using 45 nm Technology in Tanner EDA tool for circuit design S-EDIT and T-SPICE for simulation (Figure 2).

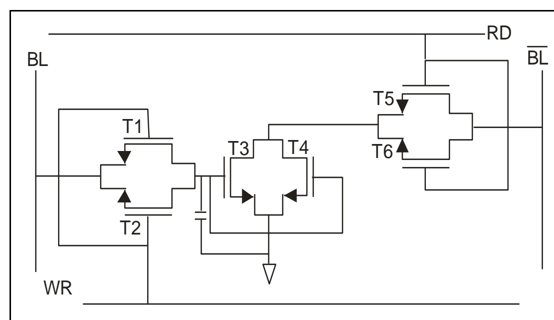

Fig. 2: *3T DRAM Using FinFET Circuit.*

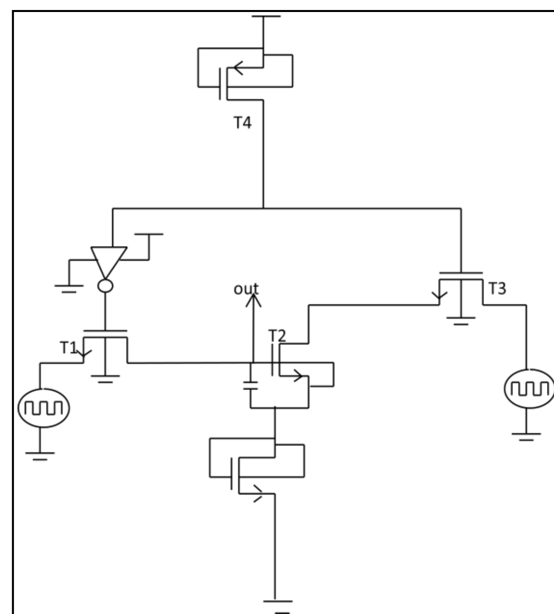

Fig. 3: *3T DRAM using MTCMOS.*

3T DRAM USING MTCMOS TECHNIQUE

MTCMOS expanded as Multi-threshold CMOS is a CMOS chip having a Transistor with multiple threshold voltage. Standby power is reduced by approaching the Pmosfet with higher threshold voltage Vth in between power supply and low threshold voltage Vth transistor for disconnecting the power supply and nMOSFET switches with higher threshold voltage Vth using in between ground and low Vth nMOS transistor for disconnecting the ground from low Vth transistor in active mode low Vth transistor can worked as low switching power dissipation and low switching.

In sleep mode the high Vth transistor of the circuit are turned off result in isolation of low Vth from supply voltage and ground by reducing sub-threshold leakage current. Multi-threshold complementary metal oxide semiconductor is a very effective circuit level technique which provides high performance and low leakage power design strategy (Figure 3).

3T DRAM USING SVL TECHNIQUE

SVL circuit is developed in three types.Type-1 shows a circuit of Upper SVL. Type-2 shows a circuit diagram of Lower SVL, and Type-3 shows the circuit diagram of combination of Upper SVL and Lower SVL. In Type-1 SVL circuit a single pMOSFET switch (p-SW) and two nMOSFET switches (n-SWs) are connected in series. The "on p-SW" is turned ON (i.e. n-SWs are connected to power supply Vdd) and the load opted in the active mode is operated, and "weekly on n-SWs" (i.e. n-SWs that are turned on) connect to the vdd and the

load circuit is in the standby mode. It should be noted that both gate and drain n-SW1 must be joined. In the similar way, the Type-2 SVL circuit, Which is named as lower SVL circuit which contains single nMOSFET switch n-SW and the two pMOSFET switches P-SWs connected in series and is connected between a ground-level power supply Vss and the load circuit. The function of the lower SVL is to supply Vss to the active load circuit through the "On n-SW" along with that to supply Vss to the load circuit through week p-SWs. A gate and drain of p-SW1 should also be connected whereas in Type-3 both upper SVL and lower SVL circuits are connected (Figures 4–6).

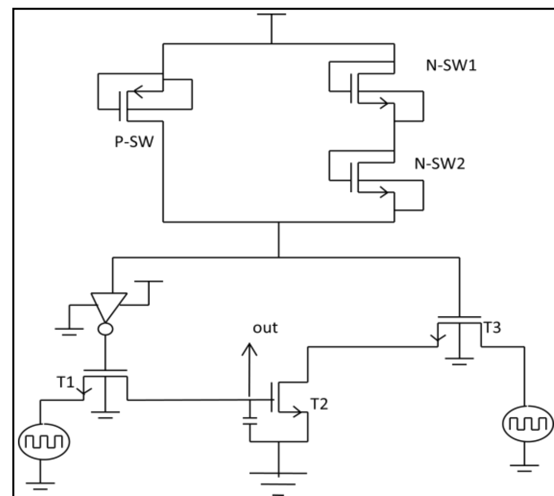

Fig. 4: *3T DRAM using USVL.*

SIMULATION AND RESULT

We have simulated and compared the operation of 3T DRAM cell; FinFET based 3T DRAM cell, 3T DRAM cell using MTCMOS technique and 3T DRAM cell using SVL technique. Its simulation results are shown in Table 1 and result compared in Figures 7–10 respectively. Simulation of operation of three transistor DRAM cell is done successfully. Power results for 3T DRAM cell is designed with Tanner EDA tool with modal file of 45nm high performance technology taken from PTM. The technique based 3T DRAM are more efficient as compare to conventional one in respect to average power, leakage voltage, leakage current and leakage power. MTCMOS based 3T DRAM was observed with least average power, leakage voltage, leakage current and leakage power with 482.4 pW, 17.4 pA and 3.9 pW respectively than any other technique.

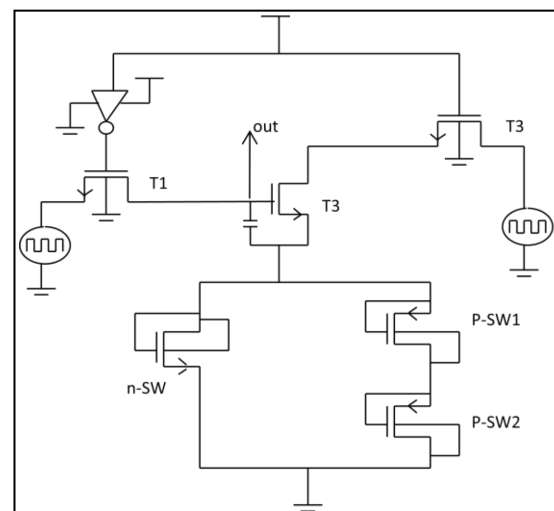

Fig. 5: *3T DRAM Using LSVL.*

Table 1: *Simulated Result Summary.*

PARAMETER	3T DRAM	3T DRAM Using FINFET	3TDRAM Using SVL Technique	Proposed MTCMOS Technique
Technology Used (nm)	45	45	45	45
Supply Voltage (V)	0.7	0.7	0.7	0.7
Average Power (n W)	4.9	2.15	1.05	482.4 pW
Leakage Current (p A)	134.4	105.3	224.2	17.4
Leakage power (p W)	214.8	9.5	550.5	3.9

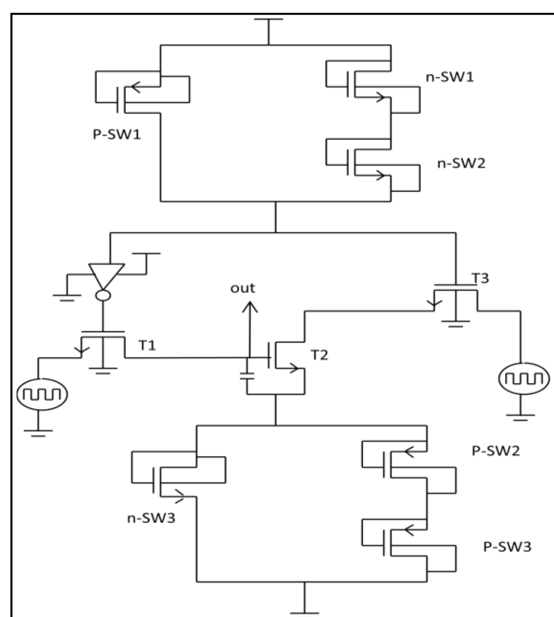

Fig. 6: *3T DRAM Using SVL.*

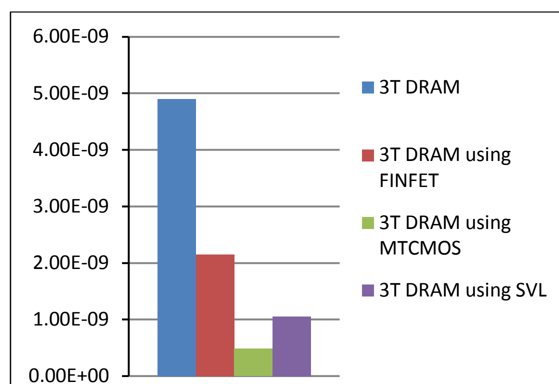

Fig. 7: *Average Power (nW).*

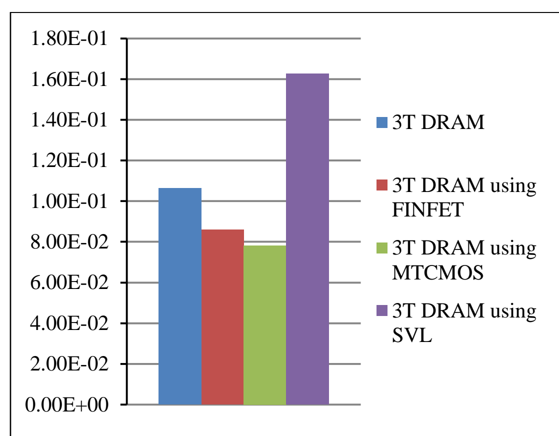

Fig. 8: *Leakage Voltage (mV).*

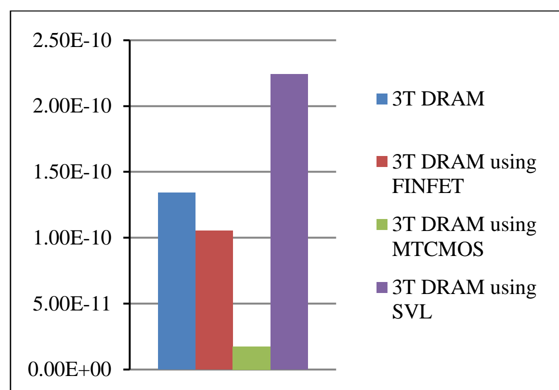

Fig. 9: *Leakage Current (pA).*

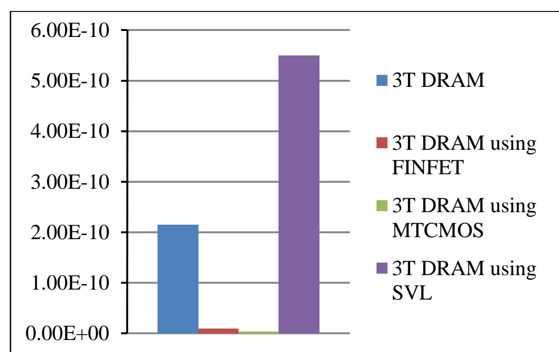

Fig. 10: *Leakage Power (pW).*

CONCLUSION

The increasing demand of large storage capacity leads towards the development of memory based devices but as the technology scaling down there is more demand of devices that are compact with low leakage current. By observing all the parameters it is concluded that FinFET CMOS technology provides low leakage and power consumption. We have investigated that the leakage current and leakage power in MTCMOS based 3T DRAM is decreases as compare to conventional 3T DRAM and 3T DRAM using other techniques. We have also observed that the efficiency of MTCMOS based 3T DRAM is higher than other 3T DRAM cell in 45 nm technologies at optimum Vdc (supply voltage).

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held at Bangkok, Thailand which was organized by the International Telecommunication Union and Government of Thailand. Madhya Pradesh Council of Science and Technology, Government of Madhya Pradesh, had provided international travel support to Mr. Khandelwal for the training. In February 2014, Mr. Khandelwal received Young Scientist award by M.P. Council of Science and Technology, Government of Madhya Pradesh, India. Recently in April 2015, Mr. Khandelwal received young outstanding person Award by the JC International Gwalior. His biography published in Marquis's Who's Who in Engineering Field, USA awarded by Marquis, 2015. In 2016, he has been shortlisted for the India TR 35 award for the year 2016 (Young Innovator Award from MIT Technology Review 35). In the same year, Mr. Khandelwal has been the recipient of the Cambridge Certificate (The International Biographical Center "CAMBRIDGE CERTIFICATE" for outstanding engineering achievement Mr. Khandelwal is a reviewer of various renowned Journals cited by Science Citation Index, Scopus etc. He is also a life member of Indian Science Congress, Government of India. His areas of research are modeling of novel semiconductor devices, and VLSI Technology, ultra-low power VLSI/ULSI Design and Technology, nanoscale memory design, digital VLSI circuit design, VHDL and FPGA implementation.

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