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Single Bit Low-Power High-Speed Full Adder

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Abstract

This paper presents a high-speed low-power full adder cells that lead to have a reduced power-delay product (PDP). A comparison against other full-adder structure as having low PDP, in terms of speed, power consumption and area of cells is carried out. This paper contains, a hybrid 1-bit full adder design employing both complementary metal-oxide semiconductor (CMOS) and transmission gate logic styles. First implemented was the design for 1 bit then extended it for 32 bit also. The circuit is implemented using Tanner EDA tools in 125 nm technology. The circuit parameters such as power, delay, and layout area were compared with the technology and compared with the existing designs such as complementary pass-transistor logic, transmission gate adder, transmission function adder, hybrid pass-logic with static CMOS output drive full adder, and so on. In comparison with the existing full adder designs, the present implementations were more significant improvement in terms of power and speed.

Index Terms: *Carry propagation adder, high speed, hybrid design, low power*

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INTRODUCTION

Full adders, one of the most fundamental building blocks of all the electronic circuit applications, remain a key focus domain of the researchers over the years. Increased usage of the Battery-operated portable devices, demand of VLSI and ultra-large-scale integration designs with an improved power delay characteristics. Energy-efficiency is most required factor for modern systems for high-performance and/or portable application designs.

Different logic styles, each having its own merits and demerits, implemented 1-bit full adder cells [1–3]. The designs, reported yet, classified into two categories: 1) static style and 2) dynamic style. Static full adders more reliable, simpler with less power requirement but the on chip area requirement is larger than its dynamic one [1,2].

Due to the rapid growth in electronic devices with constraint of power, it becomes an analytical challenge as well as a competitive task to design low-power consumption, high performance and small chip area of a circuit to increase product competitiveness for integrated circuit designers. The full adder (FA) is interpreting as the most significant and essential building block in an arithmetic unit of electronic devices in today's competitive markets. Therefore, it becomes a more complicated issue to design a high-speed, low-power FA (LPHS-FA) occupying a small chip area. Circuit design and analysis of proposed full adder: For performance improvement and circuit complexity reduction, Boolean functions of the full adder are represented as:

$$So = H'Ci + HC' \quad (1)$$

$$Co = HCi + H'A \quad (2)$$

Where, $H = A \oplus B$ and $H' = A \odot B$. A low-power, high-speed full adder is made up of an XOR–XNOR module and a sum module and a carry module. The XOR–XNOR module generates the outputs H and H' for performs XOR and XNOR logic operations on inputs A and B. Subsequently, H and H' both are applied to the sum and the carry modules for generation of sum output So and carry output Co[4].

LITERATURE SURVEY

Aguirre-Hernandez and Linares-Aranda [5] design two low-power, high-speed full-adder cells with an alternative internal logic structure and pass-transistor logic styles which reduces

power-delay product (PDP). The internal logic structure has been taken as the standard configuration in most of the developed for the 1-bit full-adder module. In this configuration, the adder module is made from three main logical blocks: a XOR-XNOR gate to obtain blocks A⊕B and $\overline{A \oplus B}$, and XOR blocks to obtain the CARRY (Co) and SUM (So) outputs.

Gang et al. [4] introduces magnetic low-power high-speed full adder. Magnetic Full Adder design is based on pre-charge sense amplifier (PCSA) circuit and logic-in memory architecture. The paper is organized writing and reading scheme used in this MFA design. Thermally Assisted MTJ Writing methods are of three types: field induced magnetization switching (FIMS), thermally assisted switching (TAS) and spin torque transfer (STT).

Three types of sense amplifier (SA) suitable for hybrid MTJ/CMOS logic circuits, they are SRAM based SA, DCM based SA, and pre-charge SA (PCSA). Pre-charge Sense Amplifier gives the best sensing reliability and power efficiency in high-speed performance. PCSA consists of pre-charge, discharge sub-circuit and a pair of inverters, act as current sense amplifier.

Following method design a magnetic full adder (MFA) consisting of PCSA, MOS logic tree and MTJ cells. The 1-bit full adder function can be given by following equations

$$\sum \quad A \oplus B \oplus Ci \tag{3}$$

$$Co = AB + ACi + BCi \tag{4}$$

Where, three 1-bit inputs A, B, Carry in (Ci) generate two 1-bit outputs SUM and Carry out (Co).

Sridharan et al. [6] present a multiternary digit (trit) adder in carbon nano tube field effect transistor design technology. This type of adder is based on a single-trit full-adder design with less complexity encoder and carry generation unit. Further, reduce the number of encoder and decoder blocks putting together with several single-trit full-adder units to aware of a multitrit-adder. The HSPICE simulation results show roughly 79% reduction in PDP for three-trit adders and 88% reduction in PDP for nine-trit adders in comparison to a direct realization.

Tung et al. [7] present carry modules that realized with multiplexers. The carry module is particularly implemented by an NMOS multiplexer. Both H and H′are applied to the NMOS multiplexer as the control signals, whereas Ci and A are the input signals to perform the operation in (2). In the structured NMOS MUX consist of two NMOS transistors, the carry signal is propagated in a highly efficient manner, but the disadvantage of weak signal level, which can be pulled up to Vdd through an energy storage technique which is combination of an inverter and a pull-up PMOS transistor. In other words, the weak signal level at C_o is inverted to '0' at C'_o to enable the pull-up transistor PMOS and the signal level at *Co* is pulled up.

In contrast, the sum module is implemented by a transmission gate (TG)-based multiplier. Both H and H′signals are applied to the MUX as control signals, whereas Ci and C′o perform the logical operation in (1). Giving Ci and C′o as the input to the multiplexer, the sum module acquires a simple structural advantage and an increases output driving capability. Use of the PTL technique in the circuit design gives rise to a simple configured and graceful FA.

Srinivasu and Sridharan [8] presents the multiternary digit (trit) multiplier design in carbon- nanotube field-effect transistor (CNTFET) technology with the help of unary operators of multivalued logic. The two full adder of Sridharan *et al.* [6] and half adder are used in the multiplier.

Design Approach of the Proposed Full Adder

The projected full adder circuits represented are having three blocks as shown in Figure 1. Module 1 and module 2 are the XNOR modules which generate the sum signal (SUM) and module 3 generates the output carry signal (Cout). Modules explained below are designed separately such that the overall circuit is optimized in terms of power, delay, and area.

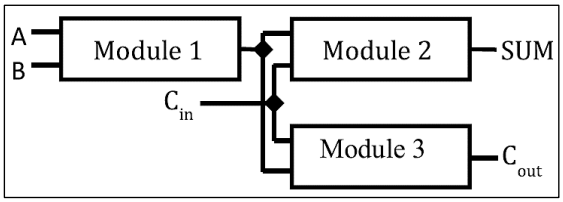

Fig. 1: *Schematic Structure of Proposed Full Adder.*

XNOR Module

In this adder circuit, XNOR module is fully dependable for power consumption of the entire circuit. Therefore, this module is designed to reduce the power to the best possible enlarge with avoiding the voltage deprivation possibility. Figure 2 shows the modified XNOR circuit, the power consumption is reduced considerably with the use of weak inverter (channel width of transistors being small) created by transistors Mp1 and Mn1. Full hang of the levels of output signals is assured by level restoring transistors Mp3 and Mn3. The modified XNOR explained in this paper offers high-speed and low-power (with suitable logic swing) compared with 6 T XOR/XNOR [4].

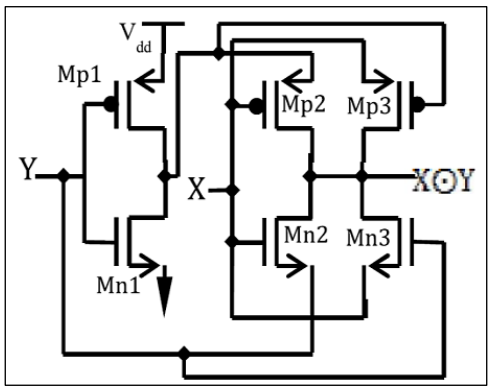

Fig. 2: *XNOR Module.*

Carry Generation Module

Proposed circuit, the output carry signal is considered by the transistors Mp7, Mn7, Mp8, and Mn8 as shown in Figure 3. The conscious use of strong transmission gates (channel width made larger) further decrease in propagation delay of the carry signal. The input carry signal (*Cin*) propagates through a single transmission gate (Mn7 and Mp7), reducing the overall carry propagation path considerably.

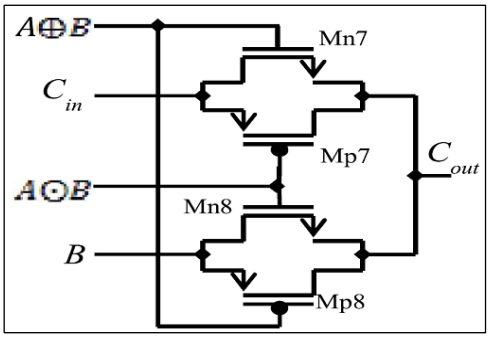

Fig. 3: *Carry Generation Module.*

Figure 4 shows the overall circuit diagram of the proposed full adder. The sum output of the full adder is designed by XNOR modules. The inverter comprised of transistors Mp1 and Mn1 generate B', which is effectively used to design the controlled inverter using the transistor pair Mp2 and Mn2. Output of this inverter is the XNOR of A and B. But it's having voltage degradation problem, this problem solved using pass transistors Mp3 and Mn3. The complete SUM function implemented using pMOS transistors (Mp4, Mp5, and Mp6) and nMOS transistors (Mn4, Mn5, and Mn6). Analyzing the full adder truth table, Carry out (Cout) generation condition has been deducted as:

If, $A = B$, then $C_{out} = B$; else, $C_{out} = C_{in}$.

The parity checked between inputs A and B as AʘB function. If both are same, then Cout is same as B, which is designed using the transmission gate realized by transistors Mp8 and Mn8. Otherwise, the input carry signal (Cin) is reflected as Cout which is designed by another transmission gate which consist of transistors Mp7 and Mn7.

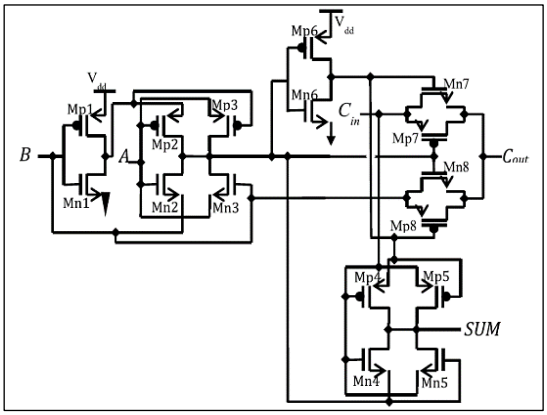

Fig. 4: *Detail Circuit Diagram of Proposed Full Adder.*

The increasing degradation in signal level causes faulty output and the circuit may failure under low supply voltages. It is likely that a single bit adder cell implemented for best performance may not perform well under operation to real time conditions. The driver adder cells may not provide proper input signal level to the driven cells in cascaded form. The inputs to the adder cell are fed through the buffers to include the effect of input capacitance and the outputs are also loaded with buffers for proper loading condition. The projected full adder is simulated using Tanner EDA test bench setup.

RESULTS

The simulation of the proposed adder carried out with 125 nm technology and compared with other adder circuits reported in [1–13]. With the aim to reduce both power and delay of the circuit, the energy consumption has been minimized in the proposed case. It was observed that the carry propagation delay enhanced by mostly sizing the transistors of the transmission gates between the paths from C_{in} to C_{out} and the power consumption minimized by mostly sizing the transistors in inverter circuits. Power consumption, propagation delay, and PDP of the proposed full adder along with that of existing full adders (from literature) are given in Table I for 125 nm technology [14–23]. Also the waveforms of the proposed adder with power are shown below in Figures 5 and 6.

The simulation results are shown below in tabular form in Table1 with the help of literature survey.

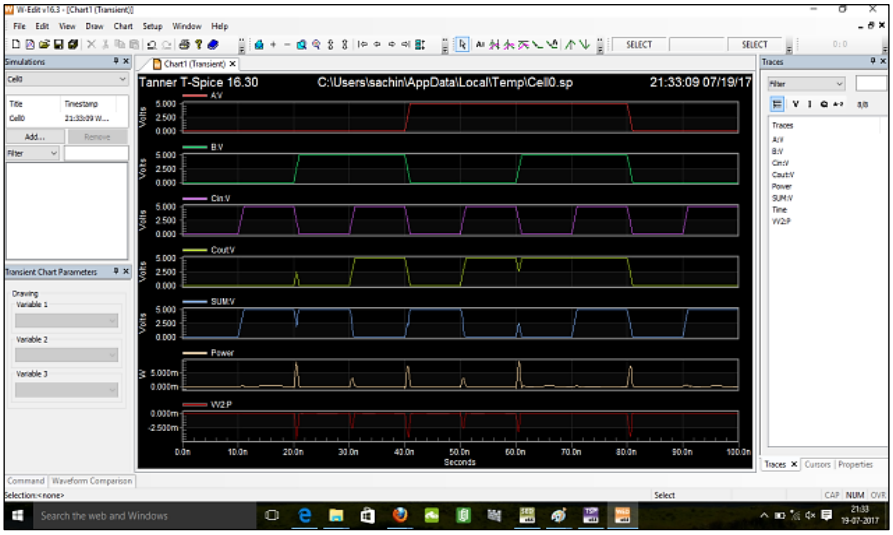

Fig. 5: *Waveform of Proposed Adder Circuit.*

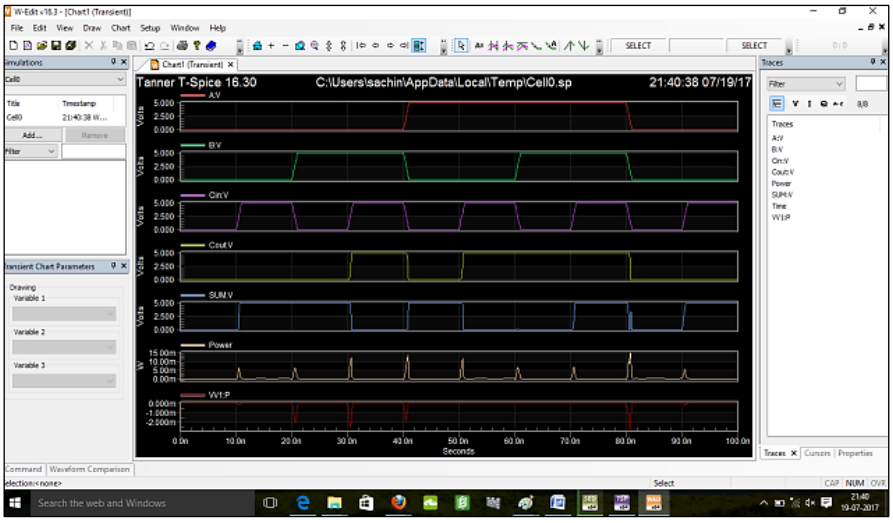

Fig. 6: *Waveform of CMOS Adder Circuit.*

Table 1: *Simulation Result for 125 nm Technology with 5V Supply.*

Sr. No.	Model	Power Consumed by input(W)			Delay (ps)
		A	B	Cin	
1.	CMOS adder	0	$2.54e^{-022}$	$3.91e^{-008}$	292.4
2.	Ripple Carry CMOS adder	0	$4.57e^{-024}$	$1.04e^{-008}$	303.2
3.	Proposed Adder	0	$2.31e^{-020}$	$-7.47e^{-005}$	225
4.	Proposed Ripple Carry	0	$-3.59e^{-019}$	$3.5e^{-005}$	240.1
5.	Proposed CLA adder	0	$-1.50e^{-019}$	$2.91e^{-005}$	231

CONCLUSION

In this paper, proposed a low-power single bit full adder design has been extended for 32-bit also. The competent coupling of strong transmission gates driven by weak CMOS inverters lead to fast switching speeds (in 125 nm technology) not including buffer. The full adder gives 20.56% improvement compared with best reported design in terms of PDP. The proposed full adder can be additionally used to implement a 32-bit carry propagation adder, having buffers at suitable adder stages (after three stages).

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