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Low-Offset High Speed CMOS Voltage Comparator using 180 nm Technology

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Abstract

A low Off-Set high-speed two-stage dynamic comparator is presented in this paper. In this circuit, PMOS transistors are used at the input of the first and second stages of the comparator. At the evaluation phase, the second stage is activated after the first stage with a predetermined delay to achieve a controllable pre-amplifier gain. Also, the first stage is turned off after the delay to reduce overall power consumption. Simulation results in 0.18 µm CMOS technology prove that the proposed circuit reduces the power consumption by a factor of two and reduces comparison time as large as 210ps in the same budget of offset voltage compared to the conventional circuit. Moreover, the offset voltage and power consumption of the comparator trades with the speed which is simply controlled by the delay of the second stage. As a result, a low-power comparator for given offset and speed requirements can be designed efficiently. This comparator generated off–Set voltage is 2 mV and power consumption is 190 µW.

Keywords: *Dynamic comparator, Low Off-set comparator, High-speed comparator, Delayed comparator*

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INTRODUCTION

Nowadays, low-power design is the main trend in the design of electronic circuits [1–10]. ADCs are integral parts of a wide range of applications such as portable devices and radios. Employing low-power high-speed ADCs is essential to heighten the overall system performance. Comparators play an important role in commonly used ADCs, such as flash and SAR ADCs. Static comparators have been used for years; however, they suffer from high power consumption and limited speed [1]. Dynamic comparators were presented to improve the speed and reduce the power consumption of the static comparators [2].

At first, single-stage dynamic comparators were proposed in which a preamplifier circuit is directly connected to a cross coupled latch circuit. These comparators provide higher speed and lower power consumption compared to the static comparators. However, they suffer from kickback noise which is due to capacitive paths from output nodes to input nodes [4]. Moreover, single-stage dynamic comparators suffer from a limiting trade-off between power consumption and speed. Two-stage dynamic comparators were presented to heal the kickback noise problem by weakening the capacitive path from the output nodes to the input nodes [4]. In these comparators the first stage, pre-amplifier stage, amplifies the input differential signal, then the second stage, latch stage, amplifies its input differential voltage until reaches V dd and Gnd [1]. As a result, the design of the pre-amplifier stage and the latch stage are independent from each other which lead to an easier design methodology in contrast to single-stage dynamic comparators.

Conventionally, in the two-stage dynamic comparators, input transistors are designed large enough to satisfy a given offset voltage. Therefore, a low offset criterion causes a high amount of power consumption due to large parasitic capacitors of the input transistors. Abbas et al. [5], proposed a comparator in which the first and second stages are connected together, to improve the speed and area. However, in this circuit higher speed trades with offset voltage and power significantly. According to Junjie and Holleman [6], a comparator is proposed working with only one clock signal to reduce

the number of transistors. Moreover, a bulk-tuned offset cancelation technique is presented which reduces the offset voltage of the comparator significantly. Therefore, for a given offset small transistors can be used that yields in lower power consumption. Unfortunately, lower power consumption is achieved at the cost of significant speed reduction. As another example, according to Stefano, et al. [7], a comparator with NMOS input transistors is proposed to achieve a high-speed behavior, although, it increases power consumption by a factor of four. Junfeng et al. [9] presented a new structure for dynamic comparators. This structure presents a common mode insensitive comparator which is favorable in the applications where the output common mode range of the DAC is as large as the voltage supply, such as the DAC reported by Ata and Sharifkhani [8]. This circuit helps to reduce power consumption, yet, achieves an acceptable offset voltage. However, it suffers from larger required area and higher kickback noise compared to the conventional method. In fact, being a direct connection between output nodes at the first and second stages, kickback noise becomes more destructive than two-stage conventional comparator. Moreover, its speed trades with power consumption for high resolution applications.

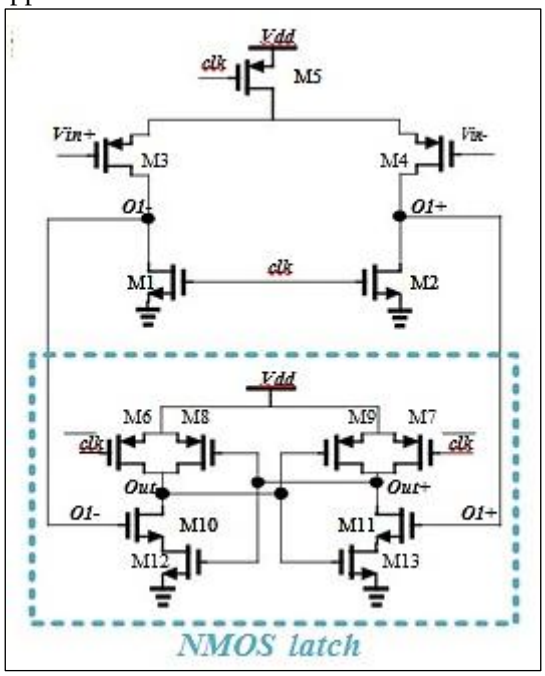

Fig. 1: *The Conventional Two-stage Dynamic Comparator [8].*

In this paper, a two-stage dynamic comparator with PMOS transistors at the input of the pre-amplifier and latch stages is proposed. This structure in addition to a predefined clocking pattern reduces power consumption. Moreover, the offset and speed trade-off is controlled efficiently. The proposed circuit provides a low-power high-speed comparator in equal offset voltage budget compared to the conventional comparator. The PMOS latch-stage of the proposed comparator provides a lower offset voltage, since PMOS transistors offer a better matching compared to NMOS transistors in CMOS technology.

CIRCUIT DESCRIPTION

Conventional Dynamic Comparator

The conventional two stage dynamic comparator and its output voltage waveforms are shown in Figure 1. As shown in this figure, the comparator is comprised of two stages, the pre-amplifier stage and the latch stage. In this circuit, the amplified input differential signal appears at the output of the pre-amplifier stage then the latch stage amplifies its input signal until its output voltages settle at V dd and Gnd. If the amplification gain of the first stage is large enough, the effect of second stage on the offset voltage is negligible [1]. In practice, the size of the input transistor is chosen large enough to satisfy a given offset criterion (Table 1). Also, the size of the latch stage input transistor is chosen carefully to satisfy the speed and strongly load the next stage (output buffers). As a result, for a given offset voltage and speed, the power consumption of the pre-amplifier stage is dominated to that in the latch stage. Moreover, the speed is limited to the speed of the latch stage in addition to the time required to charge the output parasitic capacitors of the pre-amplifier stage to an NMOS voltage threshold (V_{thn}). In fact, during the evaluation phase the second stage remains off until the output voltages of the first stage become large enough to turn on NMOS input transistors of the latch-stage.

In the second stage of the conventional comparator, NMOS transistors are used at the input, (i.e., M10 and M11 in Figure 1). The NMOS transistors are used to provide a delay for the latch stage. This delay helps to increase the gain of the pre-amplifier stage, thus,

reduce the effect of the latch-stage on the offset voltage. Unfortunately, this delay is uncontrollable and fixed to a value which is equal to the time required to charge the output parasitic capacitors of the pre-amplifier stage to V_{thn}. Moreover, this delay may put the input PMOS transistors of the pre-amplifier stage to triode region during the evaluation phase then reduce the pre-amplifier gain. This situation takes place when the common mode voltage of the input signals is low, close to Gnd.

Proposed Dynamic Comparator

The proposed circuit is shown in Figure 2. PMOS latch is used at the second stage of the comparator. The reset phase is the same as that in the conventional circuit. At the evaluation phase, the pre-amplifier stage amplifies the input differential signal within a predetermined period of time. Then the latch stage is activated to amplify its input differential signal. Simultaneously, the current source of the first stage (M5) is deactivated to reduce the power consumption of the first stage which is the main source of total power consumption. The control signals are implemented using a delay line based controller [10]. Instructively, the proposed comparator is robust to overlapped control signals, since overlapped signals only affect the power consumption slightly and have no effect on the precision.

Fortunately, the lower Low Off-Set consumption of the pre-amplifier stage let us design the input transistors (M3, M4) large enough to achieve a high pre-amplification gain without being worry about the high power consumption of the first stage. As a result of high gain of the pre-amplifier stage, the delay of the latch stage is reduced. Moreover, at the beginning of the latch stage operation, the common mode voltage of the pre-amplifier output nodes is small enough to strongly activate the input PMOS transistors of the latch stage. Therefore, the speed of the comparator increases without power consumption or speed reduction penalties. Consequently, the proposed comparator provides low-power high-speed benefits with an acceptable offset voltage. The proposed method can be extended to NMOS pre-amplifier and latch stages to achieve a higher speed at the expense of larger offset voltage, (i.e., a comparator with NMOS transistors at the input of the pre-amplifier and latch stages).

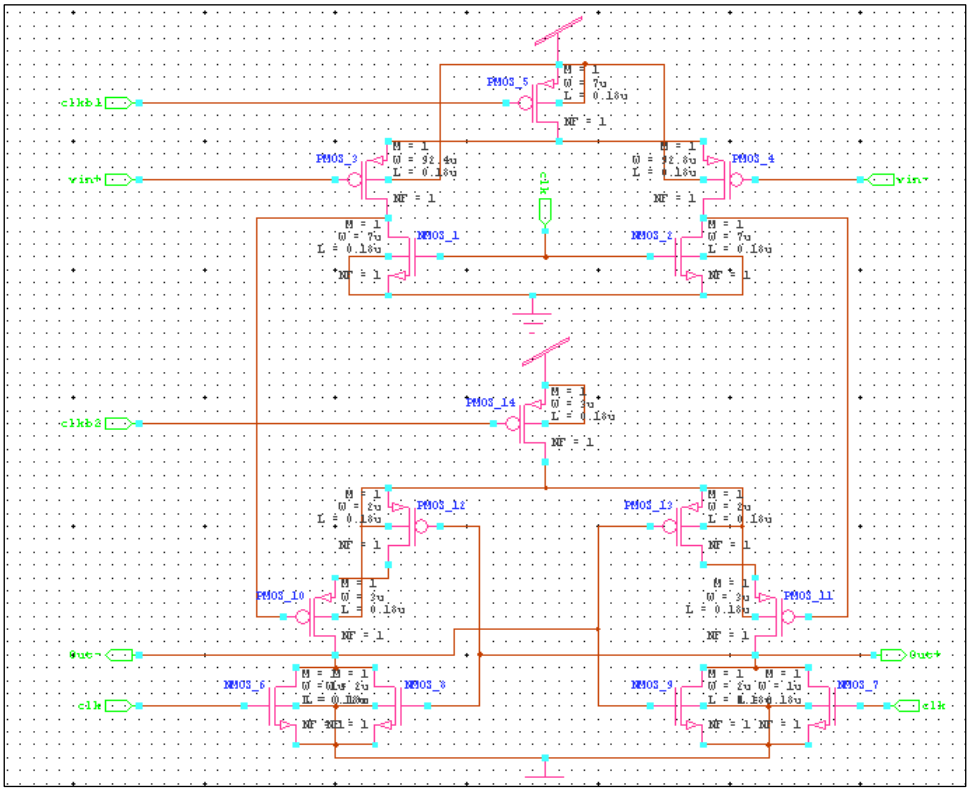

Fig. 2: *The Proposed Two-stage Dynamic Comparator.*

SIMULATION RESULTS

Input as Sine Wave

The input is sine wave in comparator are given the input signal is sine and the output of the comparator are generated pulse wave. Comparator are compare two input signal and with reference signal. This comparator are generated pule signal by two input signal. Sine wave and pulse are shown in Figure 3.

Propagation Delay for the Comparator

By definition propagation delay is the time required for the change in output with respect to the change in input. The speed of comparator depends on propagation delay; propagation delay and speed are inversely proportion to each other. If the propagation delay is higher, speed of the comparator will be lower and vice-versa. The propagation delay has founds in Figure 4 i.e. 120 ps.

Offset Voltage

Offset voltage is defined as the output voltage changes as the input difference crosses the zero. Then if the output voltage did not change up to the time the input dissimilarity could be explained as the output offset voltage as in Figure 4. This type of offset voltage could not create the problem if this offset would be predicted, but it changes arbitrarily from circuit to circuit. Cause of the offset voltage can be condensed but cannot be removed totally. The simulation result shows 2 mV offset voltage for 180 nm technology.

Figure 5 presents the offset voltage of the proposed comparator versus the delay of the latch stage. Obviously, 120ps delay is long enough to achieve the minimum offset voltage. Therefore, the delay of the second stage is chosen 150ps. In fact, additional 30ps delay (150 = 120 + 30) is considered to cover non-ideal effects, such as parasitic capacitors. Figure 4 presents an instructive observation about the benefits of the proposed comparator. This figure suggests that 120ps delay is long enough to achieve the minimum offset voltage of this comparator. However, the uncontrollable delay of the conventional comparator is far longer than 120ps. Also, the delay of the conventional comparator depends on its input common mode voltage of the comparator which is variable, thus, further deteriorates power consumption, delay, and offset voltage of the conventional comparator.

ICMR (Input Common Mode Range)

ICMR is the input common mode range. This is the range of input common mode voltage over which the comparator works normally. Generally this is the range where all transistors remain in saturation, so constant current flows during this| range. The simulation result shows the input common mode range for –0.1 to 0.12 V for the 180 nm technology as described in Figure 6.

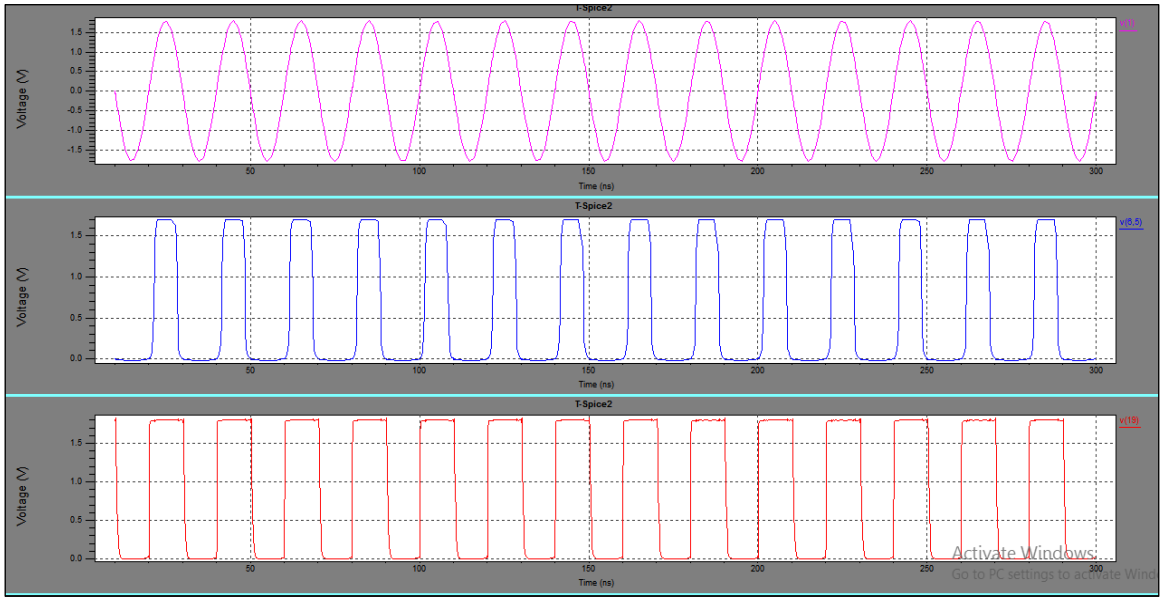

Fig. 3: *Input Sine Wave.*

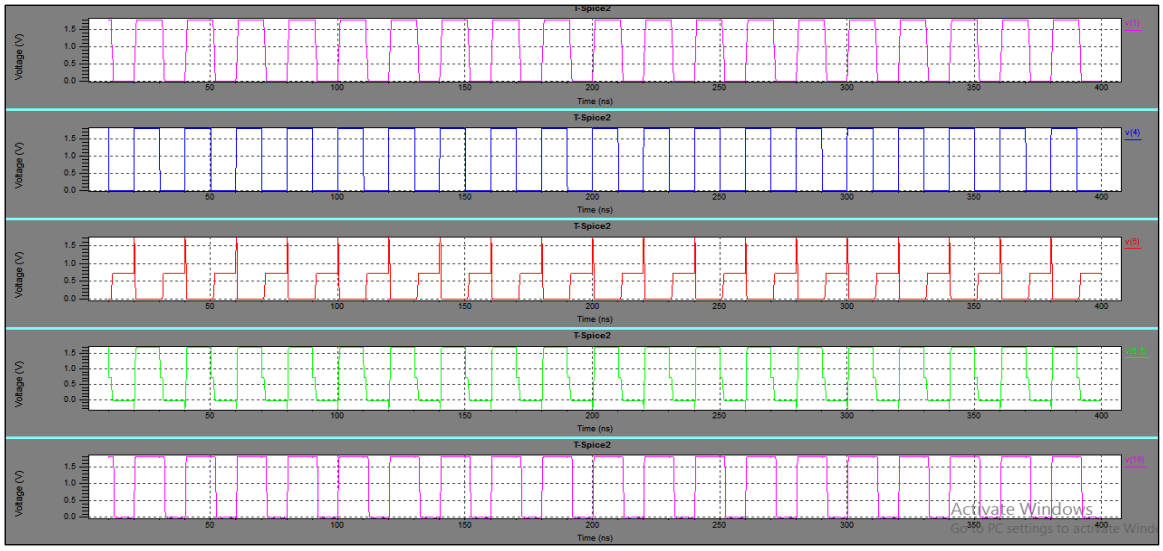

Fig. 4: *Propagation Delay.*

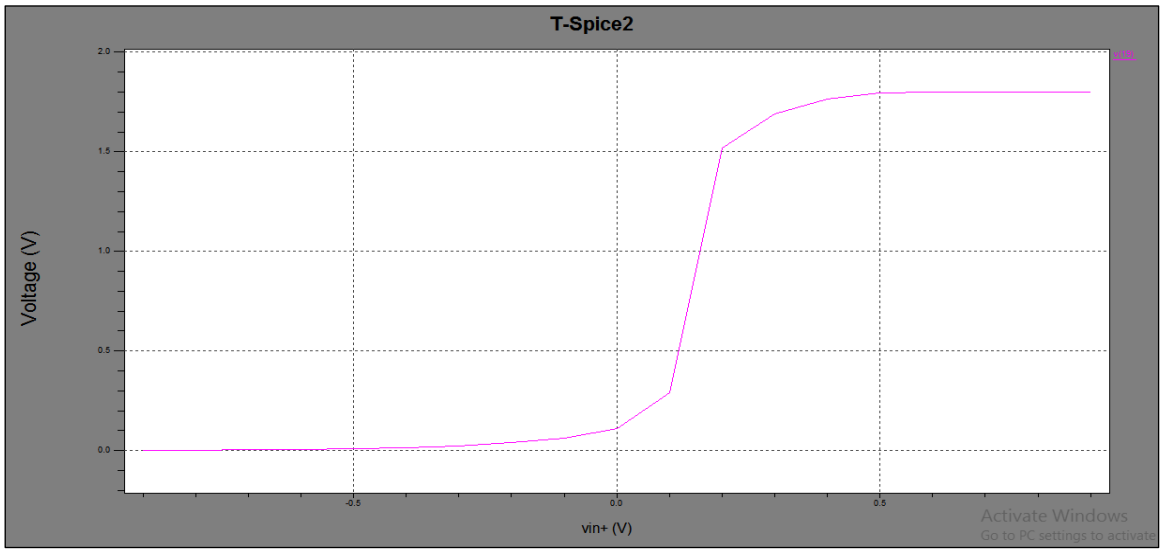

Fig. 5: *Offset Voltage.*

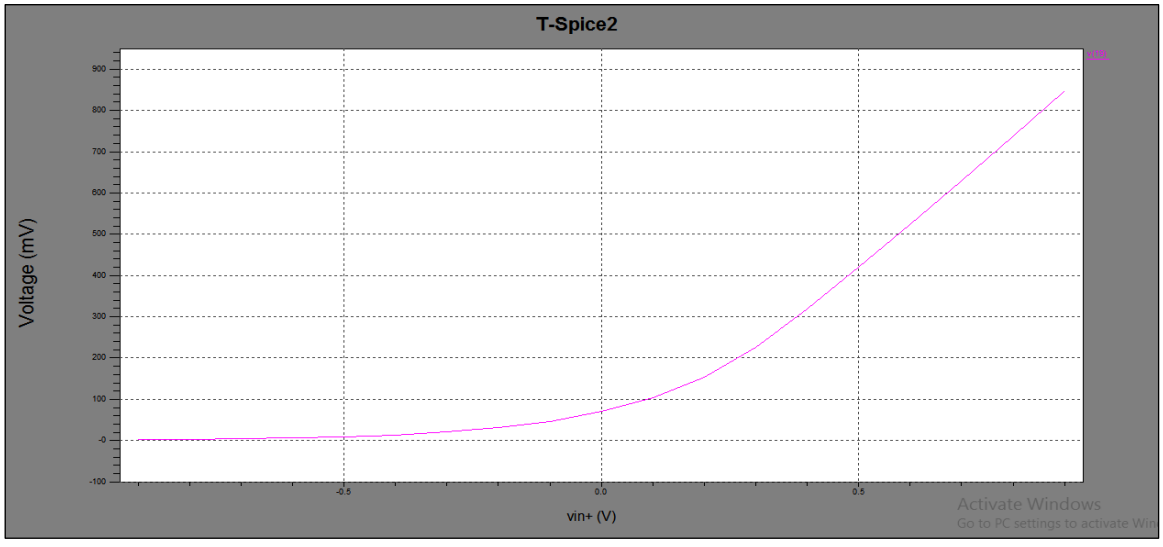

Fig. 6: *ICMR (Input Common Mode Range).*

Table 1: *Transistor Sizing of the Proposed Comparator.*

Transistor ID	Width of Transistors (um)
M1,M2,M5	7
M3,M4	92.4
M6,M7	1
M8,M9,M12,M13	2
M10,M11,M14	3

Figure 6 presents the power consumption of the comparators versus input common mode voltage. The power consumption is obtained under the condition of 500 MHz clock frequency and 1 mV input differential voltage. The proposed circuit offers the lowest power consumption while it provides an acceptable offset voltage and speed. However, the circuit proposed in consumes significant amount of power consumption. This circuit consumes more than 450% power consumption to speed up the comparator by about 52% compared to the conventional circuit.

Table 2 compares the proposed circuit with other methods. The proposed circuit reduces power consumption by 52% compared to the conventional circuit with a speed enhancement of 76:2%. The proposed method of Junjie and Holleman [6] reduces the offset voltage at the cost of very low speed and the method proposed by Stefano et al. [7] speed up the comparator with a large overhead of power consumption. Nonetheless, the proposed circuit provides a controllable low-power high-speed comparator.

Table 2: *Comparison of the Proposed Circuit with Other Circuit.*

	Conventional	[6]	[7]	[9]	Proposed
Clock Frequency	2.1 GHz	33 MHz	1 GHz	1.25 GHz	3.7 GHz
Offset (mV)	2.5	0.056	5.62	7.78	2
Power (μW)	435	766	-	600	230
Technology	0.18 μm	0.5 μm	90 nm	130 nm	0.18 μm

CONCLUSION

A two-stage dynamic comparator is presented. In this circuit, PMOS latch with a predetermined delay is used to achieve a small amount of offset and improves the speed. Also, this delay limits the voltage variation at the output nodes of the pre-amplifier stage. Therefore, the power consumption of the proposed comparator is reduced by a factor of two while the speed is improved by 76.2% compared to the conventional comparator. Simulation results in the same budget of offset voltage confirm that the proposed comparator provides a fast low-power comparator with an acceptable offset voltage which is suitable for high-speed high-resolution applications. The simulation results allow the circuit designer to fully explore the tradeoffs in comparator design such as speed, power and offset voltage.

REFERENCES

1. Razavi Behzad, Bruce A. Wooley. Design techniques for high-speed, high-resolution comparators. *Solid-State Circ, IEEE J.* 1992; 27(12): 1916–1926p.
2. Cho Thomas Byunghak, Paul R. Gray. A 10 b, 20 Msample/s, 35 mW pipeline A/D converter. *Solid-State Circ, IEEE J.* 1995; 30(3): 166–172p.
3. Khorami A, Sharifkhani M. One-dimensional adiabatic circuits with inherent charge recycling. *Electron Lett.* 2015; 51(14): 1056–1058p.
4. Figueiredo Pedro M, Joao C. Vital. Kickback noise reduction techniques for CMOS latched comparators. *Circ Syst II: Express Briefs, IEEE Trans*. 2006; 53(7): 541–545p.
5. Abbas Mohamed, *et al.* Clocked comparator for high-speed applications in 65nm technology. *Solid State Circuits Conference (A-SSCC),* 2010 IEEE Asian. IEEE, 2010.
6. Lu Junjie, Jeremy Holleman. A low-power high-precision com-parator with time-domain bulk-tuned offset cancellation. *Circ Syst I: Regular Papers, IEEE Trans*. 2013; 60(5): 1158–1167p.
7. D'Amico Stefano, *et al.* A 7.65-mW 5-bit 90-nm 1-Gs/s folded inter-polated ADC without calibration. *Instrum Measure, IEEE Trans*. 2014; 63(2): 295–303p.
8. Khorami Ata, Mohammad Sharifkhani. Zero-power mismatch-independent digital to analog converter. *AEU-Int J Electron Commun.* 2014; 69(11): 1599–1605p.

9. Gao Junfeng, Guangjun Li, Qiang Li. High-speed low-power common-mode insensitive dynamic comparator. *Electr Lett.* 2015; 51(2): 134–136p.
10. Van Elzakker Michiel, *et al.* A 10-bit charge-redistribution ADC consuming 1.9 W at 1 MS/s. *Solid-State Circ, IEEE J*. 2010; 45(5): 1007–1015p.
11. Khorami Ata, Mohammad Sharifkhani. Elimination of the effect of bottom-plate capacitors in C-2C DAC using a layout technique. *Microelectr J*. 2015; 46(12): 1275–1282p.

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